RADEON™ 9800 Series Databook

Technical Reference Manual
Rev 1.1

P/N: CHS-215R9800-11

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Chapter 1
Introduction

1.1 About this Manual

This manual is part of a set of reference documents which provide information necessary to design products built around the RADEON™ 9800 series of GPUs.

The electrical and thermal characteristics described in this document are specific to the RADEON 9800 manufactured using TSMC's 0.15µm process, which has voltages from 1.2V to 1.8V core, 3.3V PCI I/O, 3.3V and 1.5V AGP, and 1.8V and 2.5 (LVTTL, SSTL_2, and 60 Ohm matched impedance) memory interface. To obtain information about how to support ATI graphics controllers, steppings, and foundries in one PCB design, contact ATI.

The remaining chapters are as follows:

Chapter 2 - Main features of the RADEON 9800.

Chapter 3 - Details about the controller building-blocks and interfaces.

Chapter 4 - Details about the pinouts and straps.

Chapter 8 - Timing diagrams.

Chapter 5 - Electrical and physical characteristics.

Appendix A - Sorted lists for the chip pinouts.

Appendix B - Revision history for this manual.

1.2 RADEON 9800 Variants

The list below will be updated if and when new variants become available.

The ATI vendor ID is 0x1002.

Table 1-1 RADEON 9800 Series Component Part Numbers

Marketing Name	Part Number	# of pixel pipes	Core/Memory Frequency*	1st/2nd Device ID
R360 bin 1 (RADEON 9800 XT)	215R9RBKA11F	8	412/365	4E4A/4E6A
R360 bin 2 (RADEON 9800 PRO)	215R9RBKA11F	8	DDR-1 378/338 MHz DDR-2 378/351 MHz	4E48/4E68
R360 Fab 6 (RADEON 9800 PRO 128-bit)	215R9RBGA11FS	8	324/250	4E48/4E68
R360 Fab 6 (RADEON 9800 PRO)	215R9RBGA11FS	8	DDR-1 378/300 MHz	4E48/4E68
R360 Fab 6 (RADEON 9800)	215R9RBGA11FS	8	DDR-1 324/250 MHz	4E49/4E69
R360 Fab 6 (RADEON 9800 SE)	215R9PBGA11FS	4	277/250	4148/4169
RADEON 9800 PRO	215R8RBKA12F	8	DDR-1 378/338 MHz DDR-2 378/351 MHz	4E48/4E68
RADEON 9800	215R8RBKA12F	8	324/290 MHz	4E49/4E69
RADEON 9800 SE	215R8PBKA12F	4	324/290 MHz	4148/4168

* These are approximate values. The actual core/memory frequencies depend on the board design and on the memory used. In addition, the granularity of the clock PLLs also determines the actual clock frequencies.

Figure 1-1. below shows how to interpret the ATI part number.

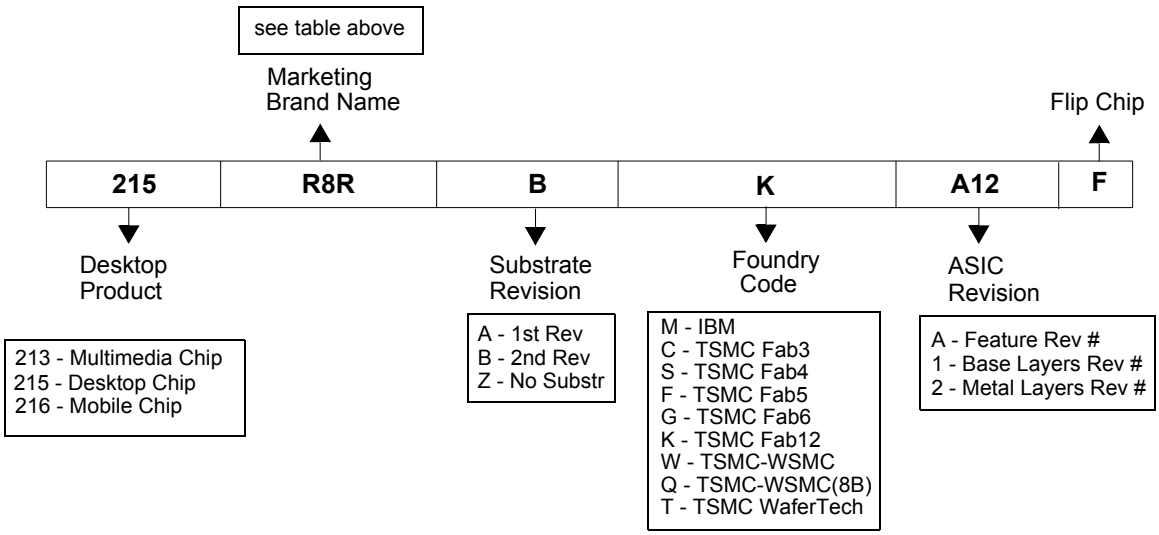

Figure 1-1. RADEON 9800 Series Part Number Code Interpretation

1.3 Branding Diagram

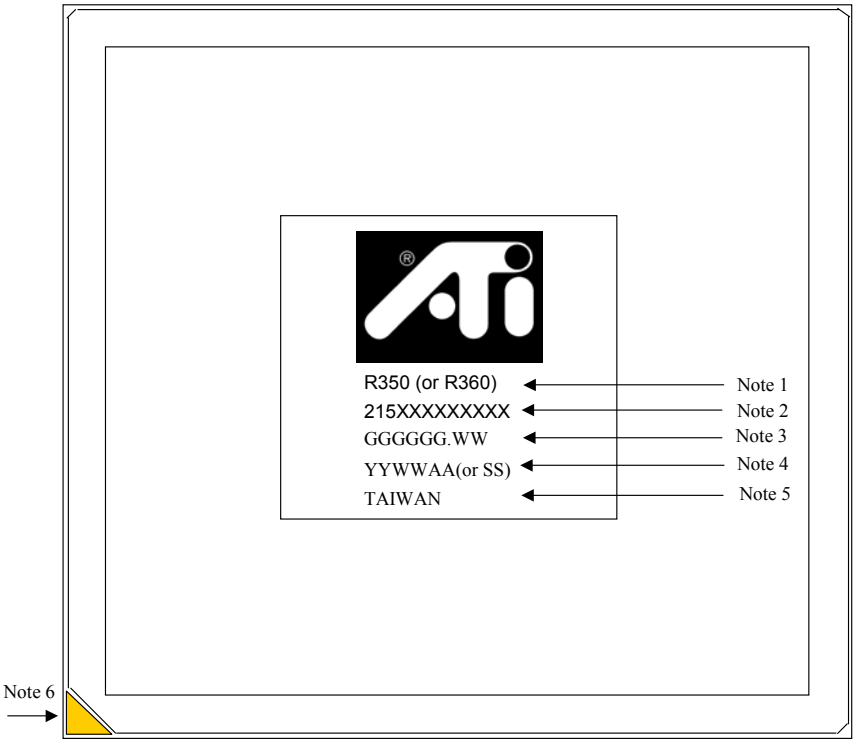

Figure 1-2. RADEON 9800 Branding Diagram

Notes:

1 ATI Marketing name

2 ATI part number. Refer to *Table 1-1, "RADEON 9800 Series Component Part Numbers," on page 2* for more information.

3 Wafer foundry's lot number.

4 Date code where YY-assembly start year, WW-assembly start week, AA (or SS)- assembly location.

5 Country of origin (Assembly site - USA, SINGAPORE, TAIWAN etc.)

6 **ASIC pin A1**

1.4 Conventions and Notations

The following conventions are used throughout this manual.

1.4.1 Pin/Signal Names

Mnemonics are used to represent pin and external strap resistors. For example the Device Select pin and the Interrupt Enable external strap are represented by DEVSEL# and ENINT# respectively.

Note: All active-low signal names are identified by either the suffix ‘b’ or ‘#’ (e.g. BLANK#, BLANKb). The two conventions ‘b’ and ‘#’ are used interchangeably.

Pins may be identified by their signal names or ball references. For multiplexed pins, only the primary function is shown but the alternate signal names will be adequately indicated in a multiplexing table.

1.4.2 Pin Types

The assigned codes for the various pin types based on operational characteristics are listed in the table below. For details about the electrical characteristics, refer to *Chapter 5*.

Table 1-2 Pin Type Codes

Code	Pin Type / Operational Characteristics
I	Digital Input
O	Digital Output
I/O	Bi-Directional Digital Input or Output
M	Multifunctional
Pwr	Power
Gnd	Ground
A-O	Analog Output
A-I	Analog Input
A-I/O	Analog Bi-Directional Input/Output
A-Pwr	Analog Power
A-Gnd	Analog Ground

1.4.3 Numeric Representation

Hexadecimal numbers are appended with “h” (Intel assembly-style notation) whenever there is a risk of ambiguity. Other numbers are assumed to be in decimal.

When the same pin name (except the following running integer) is used for pins that have identical functions (e.g. AD0, AD1, etc.), a short-hand notation is used to refer to all of them, i.e., AD[31:0] refers to AD0, AD1,..., and AD31.

The same short-hand notation is used to indicate bit occupation in a register. For example, SUBSYS_VEN_ID[15:0] refers to the Product Type Code field that occupies bit positions 0 through 15 within the 16-bit vendor ID register in PCI configuration space. No confusion is expected as the difference should be obvious by context.

1.4.4 Acronyms

Standard acronyms used in the literature are presumed known and will not be explained. When in doubt, the reader can refer to the following table for a quick check. Less frequently used or ATI-specific acronyms will have the full definition alongside in parenthesis when they appear for the first time in the document.

Table 1-3 Acronyms

Acronym	Full Expression
AGP	Accelerated Graphics Port
ATPG	Automatic Test Pattern Generation
ATSC	Advanced Television Systems Committee

Table 1-3 Acronyms (Continued)

Acronym	Full Expression
BGA	Ball Grid Array
BIOS	Basic Input Output System. Initialization code stored in a ROM or Flash RAM and used to start up a system or expansion card.
BIST	Built In Self Test.
bpp	bits per pixel
CRC	Cyclic Redundancy Check
CRT	Cathode Ray Tube
D3D	Direct Draw 3D. A Microsoft standard.
DAC	Digital to Analog Converter
DDC	Display Data Channel. A VESA standard for communicating between a computer system and attached display devices.
DDR	Double Data Rate
DFP	Digital Flat Panel. Monitor connection standard from VESA.
DPM	Defects per million
DTV	Digital TV
DVI	Digital Video Interface. Monitor connection standard from the DDWG (Digital Display Work Group).
DVS	Digital Video Stream
DX9/DX8.1	DirectX 9/DirectX 8.1. A Microsoft standard.
EPROM	Erasable Programmable Read Only Memory
FIFO	First In, First Out
HDTV	High Definition TV. The 1920x1080 and the 1280x720 modes defined by ATSC.
I^2C	Bus Protocol (Philips Specification)
DCT	Discrete Cosine Transform
JTAG	Joint Test Access Group. An IEEE standard.
LOD	Level of Detail
MB	Mega Byte
MPEG	Motion Pictures Experts Group. Refers to compressed video image streams in either MPEG-1 or MPEG-2 formats.
NTSC	National Television Standards Committee. The standard definition TV system used in North America and other areas.
PAL	Phase Alternate Line. The standard definition TV system used in Europe and other areas.
PCI	Peripheral Component Interface
PEROM	Flash Programmable and Erasable Read Only Memory
PLL	Phase Locked Loop
POST	Power On Self Test
ROP	Raster Operation
SDRAM	Synchronous Dynamic RAM
SGRAM	Synchronous Graphics RAM
TMDS	Transition Minimized Differential Signaling
UV	Chrominance (also CrCb). Corresponds to the color of a pixel.
VBI	Vertical Blank Interval
VESA	Video Electronics Standards Association
VIP	Video Interface Port
YPbPr	A three signal analog interface method for display data. Similar to YUV. Also known as "component video".
YUV	The method of video signal color encoding. Includes luma (Y, black and white component) and chroma (UV, color component)

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Chapter 2
Features Overview

2.1 Compatibility with RADEON 9700

RADEON 9800 is pinout and footprint compatible with RADEON 9700.

2.2 Major Features

- Turbo charged performance.
- Second generation Cinematic Architecture.
- SMARTSHADER™ 2.1 -- Enabled by new F-Buffer technology -- Support for Unlimited Shader Instructions.
- SMOOTHVISION™ 2.1 -- Optimized memory controller improves performance of AA & AF at high resolutions.
- HYPERZ™ III+ -- Optimized Z Cache for enhanced performance of shadow volumes.

2.3 Host Bus Support

- Comprehensive AGP support, including 8X, 4X, 2X and 1X modes of operation, Sideband Addressing, AGP Texturing (Execute mode), and support for both AGP reads and AGP writes.
- AGP fast write support.
- Complete PCI bus master and slave.
- Supports a standard, PCI 33 Specification where signal voltages do not go above 3.3V and also supports PCI 66 implementation.
- Implements a two function device to provide multi-monitor support in Win2000.

2.4 Host Data Path

The RADEON 9800 host data path supports the following tiling formats:

- Macro-tiled with pitches up to 32Kbytes and 2Kbyte surface alignment.
- Micro-tiled 32 bit.
- Micro-tiled 16 bit 8x2 pixels.
- Macro-linear.
- Micro-linear.

HDP also supports all combinations of different macro and micro tiling types. e.g. macro-linear and micro-tiled 32, or macro-tiled and micro-tiled 16.

2.5 Desktop Display

2.5.1 Display Pipes Features:

- Dual independent CRTCs and display pipes running up to 400 MHz pixel clock.
- Each CRTC capable of up to 4096 wide by 4096 high active display. With 8k x 4k totals including horizontal and vertical retrace.
- Primary display pipe supports full VGA feature set.
- Primary display supports ratiometric expansion of all source display modes up to 1600 pixels wide onto any panel size.
- Automatic ratiometric expansion in all display modes, including XVGA mode.
- Automatic panel centering in all display modes, including XVGA mode.
- HW cursor per display pipe. Operates in monochrome, color XOR mixed and color alpha blended modes up to 64x64 pixels.
- 128x128 monochrome HW icon per display pipe. Used for mobile applications.

2.5.2 Overlay/Scaler Features:

- One overlay/scaler that can be coupled to either display pipe.
- 1920 x 2 line or 960 x 4 line source data buffers (if at 16bpp).
- Up to 4x4 tap filtering.
- 2:1 horizontal pre-downscaling.
- Adaptive de-interlacing when 4 vertical lines available and not large vertical downscale.
- Frame rate conversion available when adaptive de-interlacing enabled (or possible).
- Fully programmable YCbCr to RGB color space conversion.
- Fully programmable 18 segment piece-wise-linear gamma correction of overlay output in RGB space.
- Overlay data mixing with graphics data using either exclusive mix (graphics or video per pixel), global alpha, or per-pixel alpha.

2.5.3 Display Output Features

- Primary internal DAC
  - Supports VGA or DVI-I.
  - Runs up to 400 MHz.
  - 3 channel DAC, 10 bit per channel.
  - Can source data from either CRTC, or from RMX unit.
  - Supports analog monitor connection detection using DAC comparators.
  - Supports stereoscopic display from either CRTC, including STEREOSYNC pin.

- Second internal DAC
  - Supports VGA or DVI-I, or NTSC/PAL/SECAM (composite or s-video), or component video (YPbPr or RGB).
  - Runs up to 400 MHz.
  - 3 channel DAC, 10 bit per channel.
  - Can source data from either CRTC, or RMX unit, internal NTSC/PAL encoder or component video encoder.
  - Supports analog monitor or TV connection detection using DAC comparators.

- TMDS support
  - Single link internal TMDS transmitter runs up to 165 MHz.
    The RADEON 9800 TMDS supports both coherent and non-coherent clocking systems. The drivers default to the non-coherent mode. However, the user can also select the operation mode (either coherent or incoherent) to optimize TMDS for best performance. TMDS performance can be optimized for DVI displays through the display driver control panel application.
    Incoherent receivers include the Silicon Image receiver and the Analog Device integrated receiver. Coherent receivers include the TI, Genius integrated receiver, Broadcom integrated receiver and Pixelwork integrated receiver.
  - Support for external TMDS transmitter up to 165MHz clock frequency. Digital interface to external TMDS transmitter with dedicated DDC, configurable as 12-bit (single link) or 24-bit (dual link) DDR bus.
  - Internal and external TMDS can work independently as two separate DVI connectors.
  - Dual hot plug detection pins for up to two DVI connectors.
  - Frame modulation for 18 bit panels. Independent on each TMDS channel in dual-head mode. Common in dual-channel mode.

- NTSC/PAL and Component Video Output:
  - Internal standard definition NTSC/PAL video encoder supporting up to 1024x768 display modes on composite or S-video outputs.
  - Component output (YPbPr) for 480i, 480p, 720p and 1080i (NTSC only).
    - No support for scaling or flicker removal to component video outputs.
    - Includes NTSC Macrovision and CGMS.
  - External Rage Theater or ITU-656 interface for external video encoder.

- HDCP ready.

2.6 Video Port

2.6.1 Video Port Features

- VIP 2.x compatible 8-bit video capture port.
- 2-bit VIP host port.
- Supports hardware MPEG-2 decoders. VIP 2.0 expects an 8 bit port to handle 75MHz streams.
- Digital Broadcast Satellite receiver.
- Supports RAGE Theater 1 & 2 video decode.
- Supports Rage Theater 1 & 2 audio features.
- 3.3V tolerant.
- Multi-media I^2C port. Independent from DDC ports.

2.6.2 Video Capture Features

- Video buffer. Data can be captured into one to four video buffers depending on the Capture Buffer Type (Field, Alt, and Frame) and Capture Buffer Mode (single, double, or triple).
- VBI. VBI data from the input stream is stored into two or four VBI buffers in double or quad buffer mode.
- ANC. ANC data from the input stream is stored into two or four ANC Buffers in double or quad buffer mode.
- Oneshot. Grabbing a field or frame of video data in continuous (regular operating mode) or oneshot mode.
- Mirroring. Video, ANC, and VBI buffers data is mirrored. The oneshot buffer can also be mirrored separately.
- New feature. Image flipping. Captured video is vertically flipped. This is useful for cameras mounted on laptops that might point towards or away from the user by flipping over.
- Horizontal downscaling. Downscale by a factor of x1, x2, or x4.
- Vertical scaling removed. Cannot scale down vertically.
- Capture Fake Field. When enabled, will skip the first field or frame depending on whether the Capture Buffer Type is in field mode or in an alt or frame mode.
- Input Streams. The models and emulator covered BT819, CCIR656, and MPEG_TRANSPORT types of input streams. The CCIR656 can contain ANC and/or VBI data. BT819 can contain VBI data.
- Clipping. Clips the vertical window by directly setting CAP0_V_WINDOW.CAP_V_START, CAP_V_WINDOW.CAP_V_END, CAP0_H_WINDOW.CAP_H_START, and CAP0_H_WINDOW.CAP_H_END.
- Ability to capture MPEG transport stream using 11 pin protocol with DVALID and PSYNC pins.
- Operation of capture port up to 75 MHz.

2.6.3 VIP Host Port Features:

- VIP 2.0 compliant
- Supports 4 independent DMA channels.

2.6.4 MM I^2C Features:

- Master only I^2C for connection to multi-media devices (tuner, audio decoder, etc.).
- Delay after acknowledge option added to improve transfer speed with slow external devices.

2.7 2D Features And Performance

2.7.1 2D Features

- 8/16/32-bpp micro-linear and 2x4 32-bpp and 2x8 16-bpp micro-tiled destination formats with or without macro-tiling.
- BitBLT Engine with source data from micro-linear surfaces with or without macro-tiling.
- Surface dimensions up to 2.5K by 2.5K pixels.

- Block Fill.
- Color Fill BLT.
- Line Draw.
- Bit Masking.
- Scissoring.
- Source Scissoring.
- ROP3 Support.
- Mono expansion.
- Source and Destination Color Keying.
- Destination Highlighting (for Mac).
- Scaled Bit Map available only through 3D pipe (a.k.a. "Stretch BLT").
- Alpha BLT and Anti-Aliased Text available only through 3D pipe.

2.7.2 2D Performance

Table 2-1 2D Performance

Operation	Performance	Description
Solid/brush fills	up to 6592MB/s	16B/clock through E2 block
Full ROP3's	up to 6592MB/s	Lower of 16B/clock and 1/3 of memory speed
Lines	up to 412Mpix/s	1 pixel per clock
Destination Invert	up to 6592MB/s	Same as ROP3

2.8 3D Features

- Two parallel 3D pipes, generating 8 pixels per cycle.
- First full DX9 part, including floating point per component at full speed.
- Support for 2xAA, 4xAA and 6xAA subsamples, with little performance loss in most cases.
- Advance AA quality algorithms, generating visuals that are superior to others with an equivalent number of samples.
- Up to 16 unique textures, sharing 8 texture addresses.
- HW Transformation, clipping and lighting rates of over 412 (R) million triangles per second.
  - Texture Coordinate Generation.
  - Vertex Blending (skinning) with 4 matrices.
  - 6 user defined clip planes.
  - 8 light support.
  - Directional & Local Lighting.
  - Full DX9 Vertex shader support with 4 vertex units.
- Primitive (Triangle) rates of up to 412 million textured, colored & fogged triangles per second.
- Maximum texture size 2048x2048.
- Reflections and Searchlights supported via multi textures.
- Cubic Environment Mapping.
- Perturbation bump mapping (Tritech method).
- MS standard texture compression (DXT).
- Robust OpenGL and Direct3D driver support.
- Hierarchical Z-buffer - reduces bandwidth and saves pixel writes.
- Z-buffer & color buffer compressions (reduces bandwidth) up to 24:1 (with fast clears).
- Fast Z and Color clears.
- 16 and 32 bit Z-buffer support.
- Narrow and wide Z accuracy, also support pixel shader generated Z or W.
- 8 bit stencil support, with primitive facing support.
- 16/32 bit w-buffer.

- Frame rate lock.
- On chip texture cache.
- DirectX Flexible Vertex Format.
- Robust 3D primitive support: points, lines, anti-aliased lines, wide lines, texture mapped lines, triangles, triangle meshes, triangle strips & fans, sprites, etc.
- Cull counterclockwise, cull clockwise, cull none/all.
- Flat, Gouraud and fill shading.
- Support for up to 3 separate colors (diffuse, specular, 3rd color) and OGL double sided lighting.
- 16 & 32 bit dithering.
- 4 bit sub-pixel and sub-texel accuracy.
- Pick Nearest, Bilinear, Trilinear, and Anisotropic texturing.
- Mip-mapping.
- Texture Magnification/Minification.
- Power of 2 texture map support with no limitations (includes mip maps).
- Non power of 2 textures without mip-maps.
- Projective texture (W/Q support).
- 3D Texture.
- Video textures.
- LOD biasing.
- Texture morphing & flipping.
- 3DWinBench texturing needs: Flat wrap texture addressing, cylindrical wrap U, cylindrical wrap V, clamp texture addressing, mirror texture addressing, texture swapping.
- Alpha transparency.
- One bit transparency.
- Chroma key.
- Fog: Fog vertex linear; Fog table linear & exponential; Fog vertex and color key; and Fog vertex and alpha.
- Color key and alpha transparency.
- Add pixel blending.
- Modulate pixel blending.
- Full DX9 Pixel Shader 2.0 support.
- Floating point component in pixel shader (96b pixels).
- Support for writing all pixel color formats to frame buffer (128b pixels to frame buffer), including floating point (32b).
- All frame buffer outputs available to texture unit for reading, including floating point.
- Displayable surfaces include (RGBA) at (8,8,8,8) or (10,10,10,2) or (10,11,11,0).
- Alpha Vertices.
- Texture lighting (alpha-decal).
- Decal texture blending.
- Decal alpha texture blending.
- Decal mask.
- Modulate mask.
- Modulate alpha texture blending.
- Draw behind the raster.
- Dedicated geometry acceleration for Direct3D and OpenGL which provides support for:
    - 4 parallel Vector / Scalar Engines capable of HW transformation, clipping and lighting rates up to 300 million vertices / primitives per second.
    - Transformation of homogeneous vertices from Object / Model Coordinates to Clip Coordinates.
    - Frustum Clipping on the Pint / Line and Triangle Primitive in Clip Coordinates.
    - Texture Coordinate Transformation for up to 6 texture, with support for 1,2,3, or 4 texture coordinates.

- Per Vertex Matrix Selects (PVMS), which provides 4 matrix id's per vertex, which selects from a set of up to 32 matrices.
- DirectX skinning, with a 4-matrix / 2-vertex Blending algorithm (used for Skinning, Morphing, Tweening).
- View volume clipping and up to six User-Defined Clip Planes.
- Guard-Band Clipping for clipping performance optimization.
- DirectX / OpenGL Texture Coordinate Generation.
- OpenGL / DirectX Directional (Infinite) Lighting with Infinites & Local Viewer. Up to 8 Lights. Includes DX8.1 color-per-vertex support.
- OpenGL / DirectX Local Lighting with Infinites & Local Viewer. Up to 8 lights. Includes Range and Spot Attenuation, and DX8.1 color-per-vertex support.
- DirectX dual cone spot lights for DirectX lighting model.
- Normal re-normalization and constant rescale for DirectX/OpenGL lighting model.
- Separate and combined accumulation of diffuse and specular colors for DirectX / OpenGL lighting model.
- Derivation of alpha through lighting model calculations or directly from input diffuse color.
- Vertex Reuse capability for performance optimization of triangle lists.
- Point Sprite Processing including User Clip Plane Support.
- OpenGL immediate mode interface with support for all OGL primitive types.
- Fully compliant DirectX 9, Shader Model 2.0, Programmable Vertex Shader (full operand and operation support) with up to 256 instructions and 256 vectors of constant store. This includes Vertex Shader Loops, Branches, and Subroutines.
- Wide range of compressed Vertex Shader input formats (Programmable Stream Format).
- Support for TRUFORM n-Patch Surfaces which provide for up to 15 discrete levels of tessellation and continuous tessellation ranging from 1.0 to 14.9.

2.8.1 Memory Support Features

- 16MB to 256MB of frame buffer memory using DDR configurations.
- 256-bit, 128-bit or 64-bit DDR SDRAM data bus.
- Single or dual rank configuration.

2.8.2 Power Management Features

- Supports version 1.0b of the ACPI Specification and version 1.1 of the PCI Bus Power Management Interface Specification (PCI PMI).
- The Chip Power Management Support logic supports four device power states - On, Standby, Suspend and Off - defined for the OnNow Architecture. Each power state can be achieved by software control bits.
- Clocks to some major functional blocks are controlled by a unique dynamic clock switching technique which is completely transparent to the software. By turning off the clock to the block that is idle or not used at that point, the power consumption is partially reduced during normal operation.

2.9 Compliance with Wassenaar Agreement

3D vector rate (as defined by the Wassenaar Agreement) is 42-56 M 10-pixel vectors/sec. (Note: This rate is the maximum for the RADEON 9800.)

Chapter 3
Functional Description

This chapter describes the major subsystems and interfaces of the RADEON 9800. To link to a topic of interest, use the following list of linked cross references:

3.1 Functional Block Diagram

The diagram below shows the major functional blocks of the RADEON 9800.

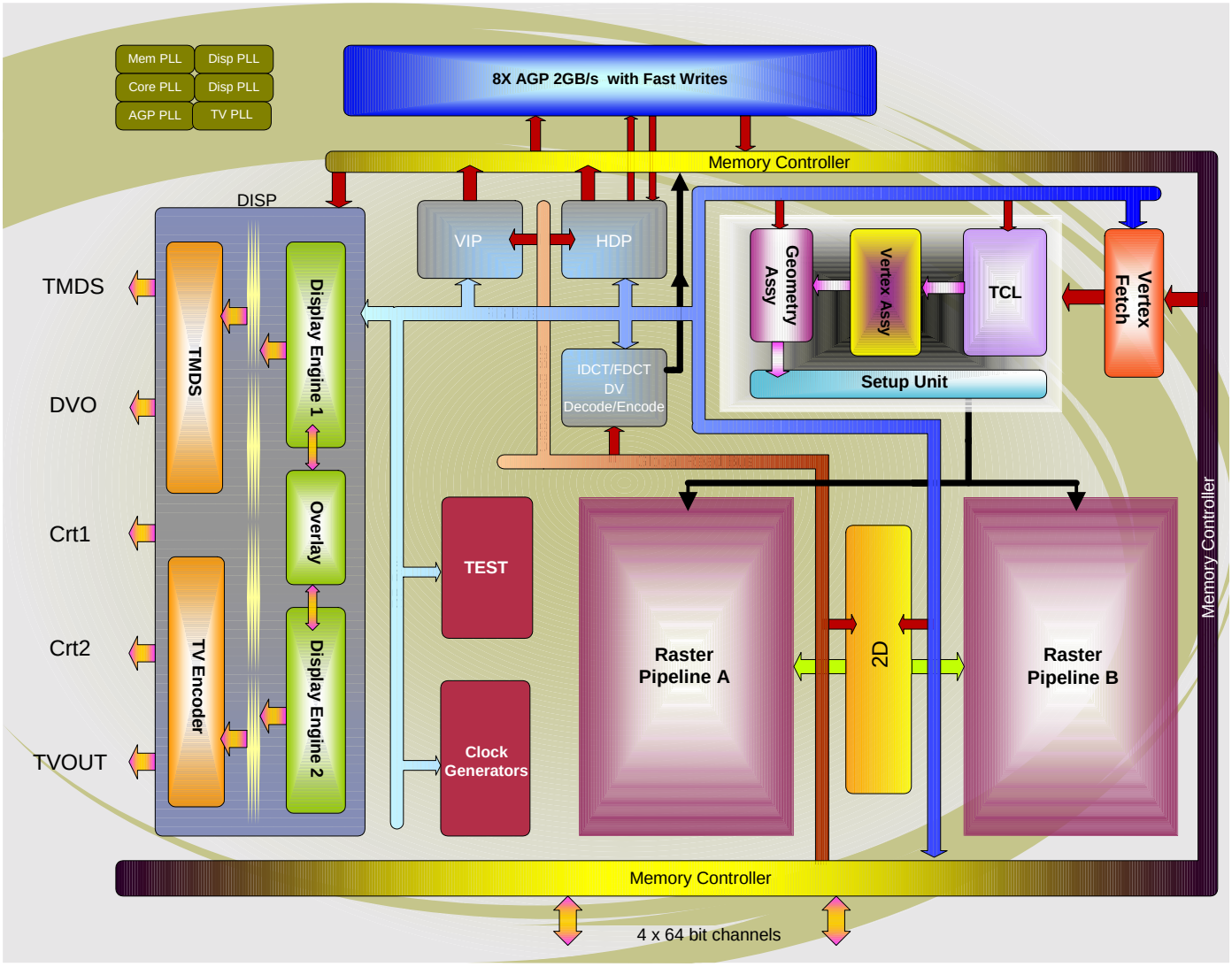

Figure 3-1. RADEON 9800 Functional Block Diagram

3.2 Display System

There are two independent display source pipelines (or CRTCs) within the display unit - display engines 1 and 2. There is also one backend scaling and overlay unit. The overlay can be attached to either display engine at any time, but cannot be attached to both at once.

All video/graphic layers (graphics, overlay, icon and cursor) are blended or mixed in the display merger 1 &2, as well as the shared graphics/video alpha blender.

The display data for display engine 1 may also optionally be ratiometrically expanded for display on fixed resolution panels.

The internal TV encoder can get input data from either internal display engine. It will optionally underscan and de-flicker the image, as well as perform the encoding or modulation that is required for the attached television type.

The internal HDTV encoder can get data from either internal display engine or the ratiometric expansion unit. It can encode either YPbPr or RGB with embedded syncs.

The internal CRT DAC can output only standard 0.7V RGB from either internal display engine.

The internal TV DAC can output standard 0.7V RGB from either internal display engine, or composite and s-video from the internal NTSC/PAL video encoder, component YPbPr or component RGB from the HDTV encoder.

The TMDS/DVO outputs can be independently driven by either display engine, or by the HDTV encoder. Dual channel DVI is only supported using external TMDS encoders on the DVO port. The HDCP unit supports either TMDS data path, but not both at once, and not for dual channel DVI.

3.3 2D Engine

The 2D engine incorporates addressing for rectangles and spans, the source data path, brush mask memory and a line draw engine. The actual ROP unit and pattern/brush memory is located in the render backend to allow the 3D and 2D engines to share the destination cache.

The source data pipe reads data from the source data buffer, aligns it to the destination, converts it into the destination format, and sends it, with the address and mask, to the render backend. The src reads inside the (0,0) to (src_scissor_right, src_scissor_bottom) region, and dest reads and writes only inside the (dest_scissor_left, dest_scissor_top) to (dest_scissor_right, dest_scissor_bottom) region.

The source data pipe block can also perform color expansion where either the background or the foreground color is selected for each pixel based on the value of each bit of the source data. In addition, there are several depalettization modes used for DIB (Device Independent Bitmap) blits and also for emulation of 3D palettized texture.

There are three color conversion modes that involve CLUT:

- 8 bit to 16 bit
- 8 bit to 32 bit (it has to be full 8888)
- 32 bit to 32 bit (gamma correction)

3.4 3D Engine

3.4.1 Geometry Assembly & Setup Engine

- Fetches vertex data for 3D primitives, supporting a number of different vertex formats, including, but not limited to: DX6 flexible vertex format, and Structure Of Arrays.
- Assembles the polygons from the primitives and vertex streams.
- Contains the post transformed vertex cache.
- Performs some of the texture operations, such as procedural textures for AA/Stippled lines, point sprites, texture coordinate wrapping, etc.
- Performs the "3D-setup" operations for triangles, rectangles, lines, and points. These operations include 1/area calculation, cylindrical wrap of texture coordinates, gradient calculations, edge parameter calculations, and culling.

3.4.2 Vertex Assembler & Processor (VAP)

The RADEON 9800 Vertex Assembler & Processor (VAP) is designed to significantly reduce CPU load and CPU memory access by taking over the processing of row vertex data from the CPU.

The VAP engine receives and fetches vertex and state data, along with primitive assembly data, to perform one of the following combination of operations:

- Pass pre-transformed/clipped/lit vertex data without modifications.
- Perform the required math necessary to transform, clip, and light user provided vertices.
- Perform texture coordinate transformation and generation.
- Perform hardware accelerated Higher-Order-Surface tessellation.
- Execute Programmable Vertex Shader programs.

When VAP is enabled, the transform process will rotate the incoming vertex positions from object to clip coordinates. The transform controller in the VAP block is also responsible for Vertex Blending and Frustum Clip code computations.

Texture coordinate transformation (Tex Xform) provides the ability to rotate a texture vector (s,t,r,q) through a 4x4

matrix. Texture Coordinates may consist of 1, 2, 3, or 4 components.

Texture coordinate generation (Tex Gen) is the process of creating texture coordinates from other data involved with the transform process. The generation of texture coordinates has the choice of: the vertex position in model or eye coordinates, the vertex normal in eye coordinates, or the computed reflection vector in eye coordinates.

The RADEON 9800 has an OpenGL Immediate Mode Interface which optimizes driver performance for Immediate Mode applications. In addition, all OpenGL primitive types are supported on the RADEON 9800.

The process of vertex lighting takes input color data and light definitions and calculates a new vertex color (diffuse and specular) based on how that vertex and normal interact with the lighting model. In general, the RADEON 9800 lighting implementation is an OpenGL lighting implementation customized to support up to 8 lights with the complete OpenGL and DirectX set of functionality. The RADEON 9800 lighting calculations are all performed in 32-bit floating point with full-range support.

The RADEON 9800 supports a fully compliant DirectX 9, shader model 2.0, Programmable Vertex Shader with full operation and operand support, 256 locations of constant store, 256 locations of instruction store, 16 input vectors, and 16 temporary vectors. Additionally, the RADEON 9800 supports a wide range of compressed Vertex Shader input formats (Programmable Stream format).

The general purpose of the clipping process is to detect any edges of a primitive which cross clip-plane boundaries and compute the intersection point in order to recreate primitives which lie completely within all clip planes. Frustum clipping clips to the view volume boundaries (typically a frustum) and the user-defined clipping allows the user to define up to 6 additional clip planes that will delete portions of the 3-D environment for purposes such as cut-away views. Guard-Band clipping is an optimization of the X (left/right) and Y (top/bottom) clipping process.

3.5 Raster Engine

The overall architecture for the RADEON 9800 consists of two pipelines. Each pipeline is able to process 4 pixels per clock with a single texture. Allocation of work between the pipelines is made based on how each graphics primitive intersects a screen based tiling pattern.

Data comes from the transform/lighting unit via multiple streams which are interleaved and used to construct complete primitives by the graphics assembly unit.

The setup unit then generates slope and initial value information for each of the texture coordinates, color or Z parameters associated with the primitive.

The resulting setup information is passed to identical raster pipeline engines which operate in parallel on generating pixel data.

The final pixel data is then written out to the video graphics memory where it will then be available for the display unit.

3.6 xDCT Engine

RADEON 9800 incorporates an integrated general purpose xDCT engine (capable of performing both forward and inverse discrete cosine transform) as well as motion compensation (MC) support for the acceleration of MPEG encoding and decoding as well as DV (digital video) decoding. The acceleration hardware is a memory to memory engine, enabling parallel operation of the xDCT and MC and high processing rates with minimal software overhead.

The memory to memory operation also increases the parallelism as well as the flexibility in load balancing between the hardware and software, which ensures that the most is made of the host processor's power. This combination of hardware acceleration decreases the loading on the host processor to significantly below that of past MC-only engines, and enables quality software DVD playback on processors which, until now, had relied on dedicated hardware decoders. It can decode both HD0 & HD1 level bitstreams for support of all 18 ATSC formats at full frame rate. In addition, the RADEON 9800 is capable of decoding 4 protected DVD streams in parallel.

The xDCT engine implements an IEEE 1180 compliant xDCT algorithm which, when combined with a dezig-zag formatter, saturation and mismatch control mechanisms, off-loads a significant portion of the MPEG decoding process from the host processor. A ring buffer is combined with control words by the host processor in a packetized format, which the advanced packet parsing engine bus masters down from system memory over the AGP bus. The ring buffer commands and xDCT coefficients are expanded and then dezig-zagged before being fed into the xDCT engine. Dezig-zagging

patterns are selectable through the register interface. There is also selection for intra/non-intra block support. The xDCT engine takes the dezig-zagged coefficients and performs a 2-D xDCT before buffering the result and sending it to the MC hardware.

The MC hardware allows for implementation of all motion compensation modes required for MPEG-2 support, with proper rounding control to meet the precision requirements of the spec. It fetches data from the frame buffer based on control information supplied by the advanced packet parsing engine on a macroblock basis, combines the data from the frame buffer with the output of the xDCT engine through a full 9-bit signed adder, and then writes the result back to the frame buffer.

3.7 Six PLL Clock Synthesizer

The internal clock synthesizer consists of six independent phase locked loops (PLLs) capable of synthesizing all required frequencies. All PLLs have been optimized for low jitter graphics applications.

- The First Display PLL generates clocks for the display system. This PLL is reprogrammed by the BIOS or driver for each display mode. It also supports clock pulling to allow GEN-locking of the display to video source material.
- The Second Display PLL generates clocks for the second display. This PLL is reprogrammed by the BIOS or driver for each display mode. It also supports clock pulling to allow GEN-locking of the display to video source material.
- The System PLL generates the clock for the 2D, 3D and xDCT engines. This PLL can generate clocks up to 412 MHz.
- The Memory PLL generates the clock for the memory (independent from the drawing engines). This PLL can generate clocks to support up to 400 MHz DDR memory interfaces (for PLL only, memory core runs at a maximum of 365MHz).
- The AGP PLL is used to generate the internal bus interface clocks. This supports an 8 times clock for AGP8X, 4 times clock for AGP 4x, or a 2 times clock for AGP 2x operation. It also can phase lock a 1 times clock for AGP 1x and PCI-66 operations. This PLL is not used in PCI-33 mode, it is automatically disabled.
- The TV PLL generates a more precise clock for TV applications.

The RADEON 9800 internal power management logic automatically stops all PLL's when in the "OFF" power state, and automatically re-starts them upon return to the "ON" state.

3.8 Video Interface Port (VIP)

VESA Video Interface Port is a multimedia bus consisting of 3 components:

- Video capture bus
- I^2C bus
- VIP host data bus

VIP is used to communicate with multimedia devices such as video decoders, MPEG decoders, analog or digital tuners, audio chips and so forth.

3.8.1 Video Capture Bus

The video capture port supports a direct connection to MPEG decoders such as the IBM-CD11, and video decoders such as Brooktree Bt829, Bt827, Bt819, Bt817, or Bt815, and Philips SAA7111/2.

The video capture port has the following features:

- Support of video stream format of BT Byte Stream, MPEG transport stream, CCIR656 and VIP 2.0.
- Capable of video data capture rate up to 75MHz.
- Hardware support for “bob and weave” and single field video capture.
- Hardware support for 3:2 pull down.
- Hardware support for VBI data capture.
- Hardware support for ANC data block capture.
- Hardware support of video mirroring and vertical flipping during capture.
- Hardware support for single, double, triple, and quadruple buffering for video capture.

- Hardware support for double, and quadruple buffering for VBI and/or ANC data.
- Hardware support for VBI horizontal downscaling.
- Hardware support of Signed UV format.
- Hardware interrupt support for video capture.

3.8.2 I^2C Bus

The I^2C is an industry standard 2-bit serial bus. The I^2C interface allows programming of peripherals such as video decoders, MPEG decoders, analog or digital TV tuners, teletext decoders, audio decoders and volume control.

Two dedicated signals, SCL and SDA, are used to drive the I^2C pins. The I^2C data transfer can be done in two modes, the software mode, or the hardware-assisted mode. In general, software controlled I^2C has higher flexibility, but yields a lower throughput because of the time involved in polling and programming the IO signals from the CPU.

Since the I^2C clock and data are open-collector signals and rely on external pull-up resistors, noise can be a factor during transition from low to high. The I^2C in RADEON 9800 can be programmed such that I^2C signals can either be driven high directly, or be pulled up by the external pullup resistor as before. Note that the driving of SCL and SDA signals is controlled separately, as this eliminates any potential problem when only one of the signals is desired to be driven high.

3.8.3 VIP Host Data Bus

The VIP host data bus is capable of supporting a maximum of four slave devices with the graphics chip being the sole master. The bus can be configured to use 2-bit data width and run up to a maximum of 33 MHz clock speed.

In the RADEON 9800, up to four busmaster channels can be supported and each channel is set to run in either direction, i.e., system or frame memory to VIP devices or VIP devices to system or frame memory. During FIFO burst mode, it is possible for the VIP driver to do a VIP register access without having to change the operating mode. Arbitration between register and FIFO transfer is hidden in the hardware. In addition, the VIP controller is capable of doing byte-aligned and dword aligned transfers, automatic interrupt polling, automatic FIFO port polling, and detect VIP slave timeout.

3.9 AGP/PCI Host Bus Interface

The system host bus interface supports both AGP 2.0, AGP 3.0 and PCI 2.2 standards. Support for AGP is by sideband addressing mode. Texture map data for 3D objects can be obtained directly from system memory. Similarly the AGP can be used to accumulate MPEG-2 playback. In these applications, AGP fetches are execute-mode fetches.

The AGP function supports pipelined reads, long reads (AGP 2.0 only), flush and fence, and writes of varying lengths. It also supports fastwrites, dual address cycles (over 4G address support), and MSI (Message Signalled Interrupts). All throttling is done in a way to prevent the bus from being put into a wait-state. The AGP function supports 1x, 2x, 4x,and 8x data transfers.

With PCI 2.2, functions such as bus control, data flow control, address/data signal generation, signal timings, and address decoding are supported. Data flow control is enhanced by a 6x64-bit write-through FIFO available in both VGA and direct memory modes.

The controller achieves zero wait-state memory read/write burst cycles with burst access. It also supports Block I/O decoding and DAC palette snooping, and a separate aperture for accessing registers.

Bus mastering between: (1) system memory and frame buffer, (2) system memory and VIP, (3) frame buffer and VIP, (4) system memory and GUI engine, and (5) frame buffer and GUI engine, allows all data transfer operations to be off-loaded from the host processor onto the motherboard chip set. The bus mastering function concurrently performs transfers on nine buffered channels, moving one “programmable amount” at a time from each of them, to prevent the other channels from starving. It also selects the highest available transfer protocol (PCI or AGP) to be used for each of the channels, and arbitrates between them.

3.9.1 AGP 2X Bus Interface

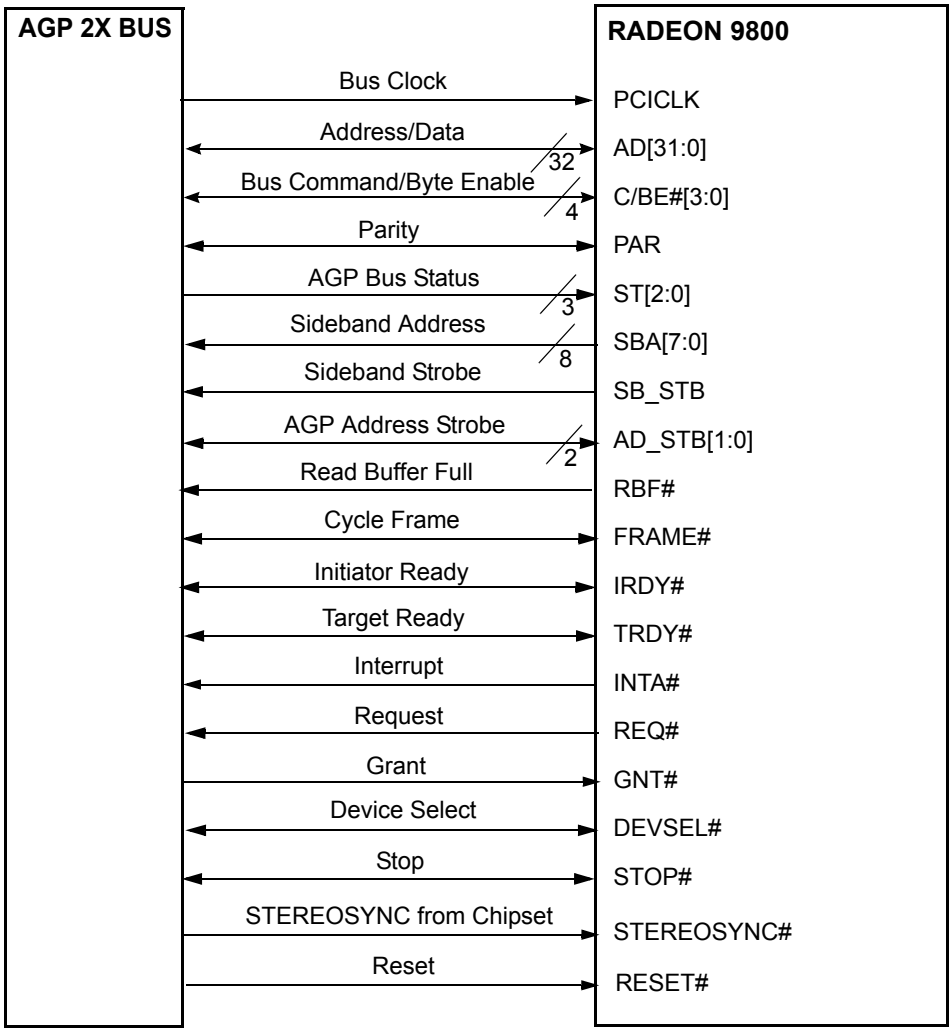

Figure 3-2. AGP 2X Bus Configuration

3.9.2 AGP 4X Bus Interface

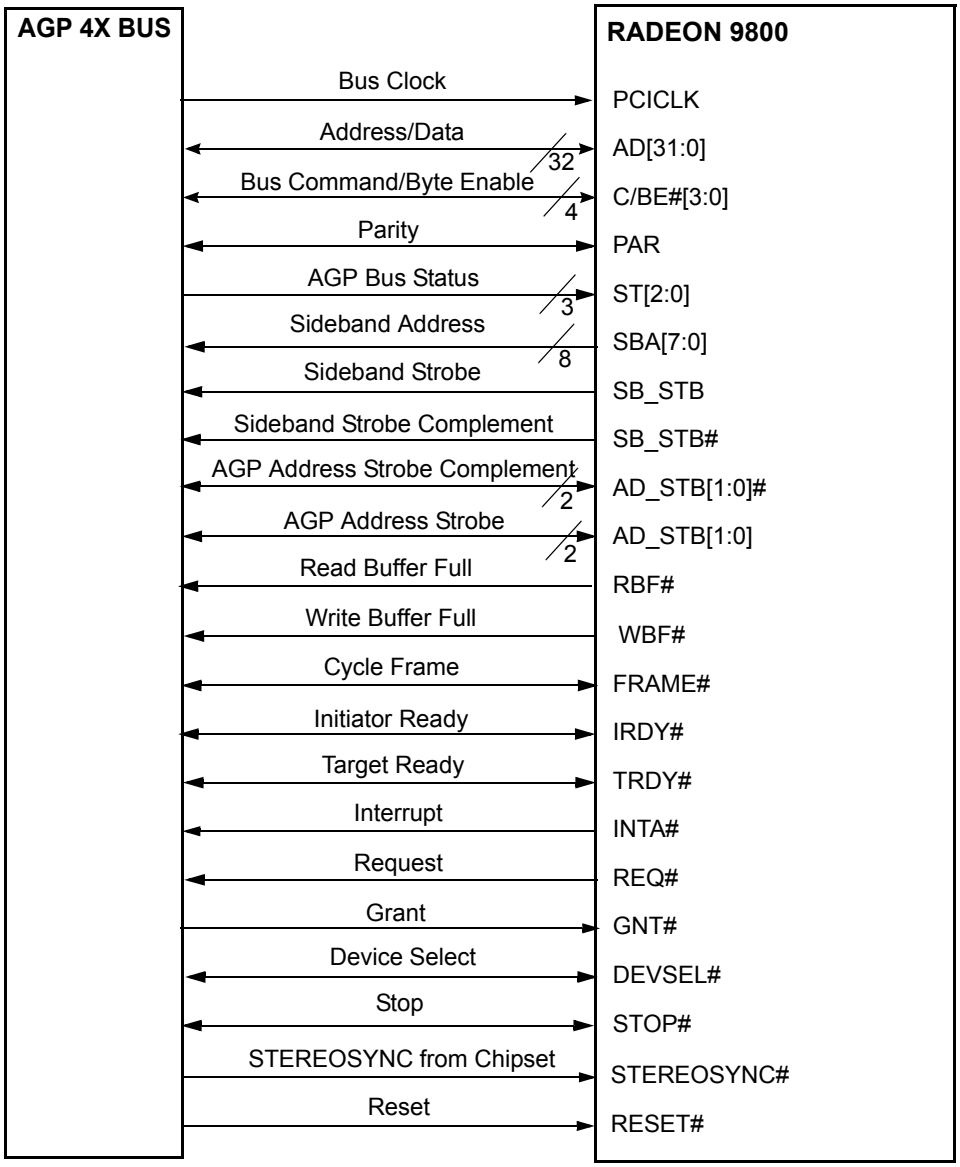

Figure 3-3. AGP 4X Bus Configuration

3.9.3 AGP 8X Bus Interface

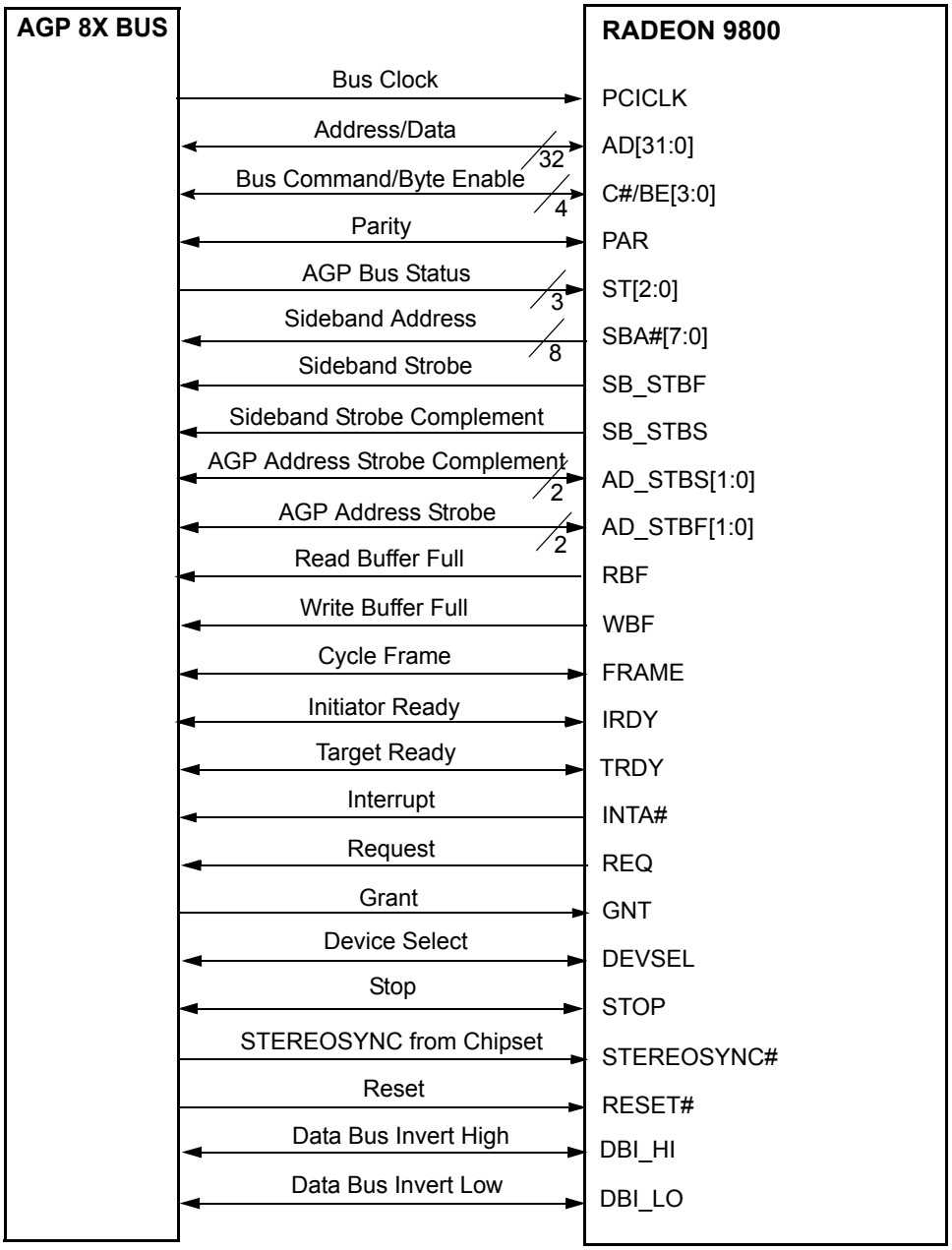

Figure 3-4. AGP 8X Bus Configuration

3.9.4 PCI Bus Interface

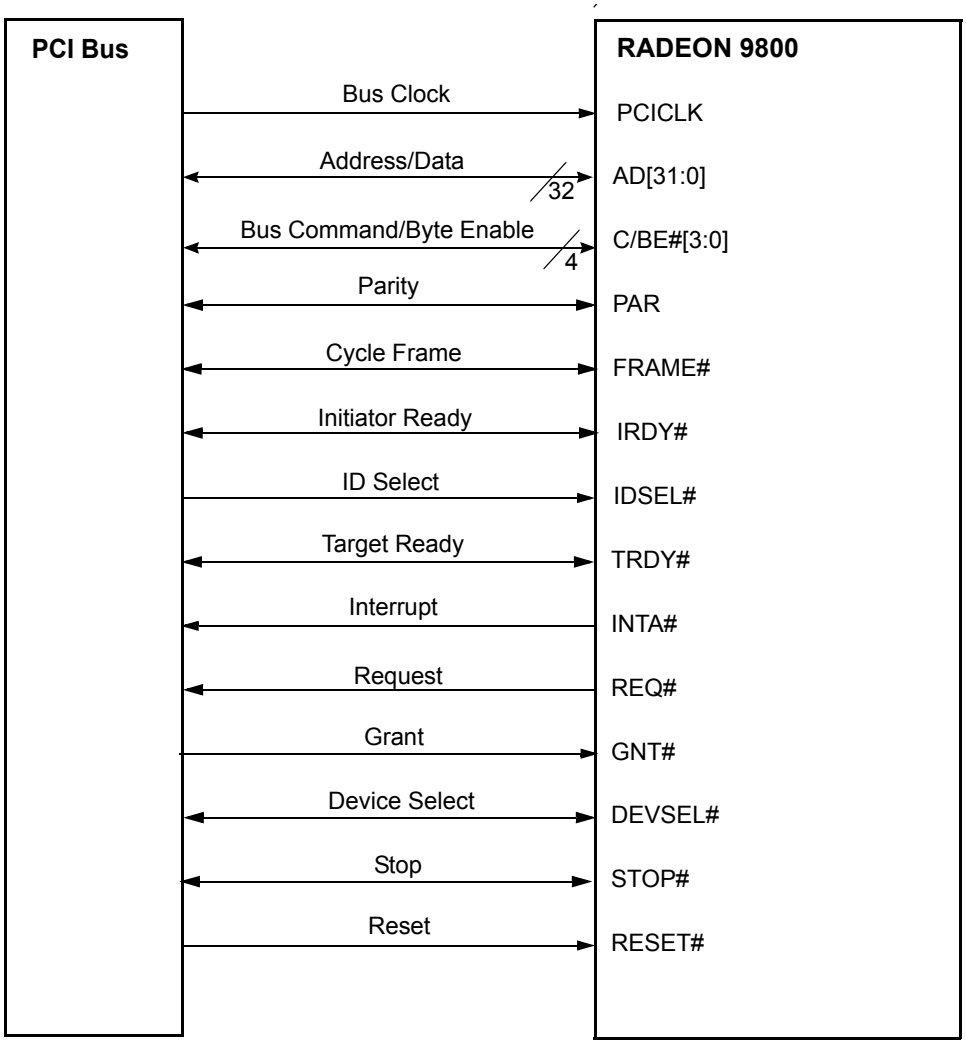

Figure 3-5. PCI Bus Configuration

3.10 Memory Interface

The memory controller subsystem arbitrates requests from the VGA graphics controller, the 2D/3D engine, the display controller, the video scaler, and the hardware cursor. Requests are serviced in a manner that ensures display integrity and maximum CPU/GPU drawing performance.

3.10.1 Memory Configurations

The memory interface for the RADEON 9800 consists of four 64-bit channels.

Memory configurations range from 16MB to 256MB (see tables below). Operating frequency is 166MHz to 365MHz for all memory types. For interfacing details on all possible memory configurations, refer to the "*RADEON Family Design Guide*" or related "*Reference Schematics*".

The block-write feature of SGRAM is not supported; either SDRAM or SGRAM may be used to achieve the same functionality.

The following memory part types are supported: SGRAM DDR, SDRAM DDR.

DDR parts with 1 strobe (QS) per byte are supported.

DDR parts with or without internal DLLs are supported.

1, 2 or 4 channels of memory are supported.

1 or 2 physical ranks of memory are supported.

To achieve full memory speed, parallel termination of the memory lines is required. Series termination of the memory lines is supported, but only at a lower speed.

The following table show the memory configurations supported for the RADEON 9800.

Table 3-1 4 Bank DDR SDRAM/SGRAM Support

Type	# of RAMs	FB Size	Memory Width	Memory Config	# of Channels	# of Ranks
1M x 32	4	16 MB	64-bit	256k x 32 x 4	1	2
1M x 32	4	16 MB	128-bit	256k x 32 x 4	2	1
1M x 32	8	32 MB	128-bit	256k x 32 x 4	2	2
1M x 32	8	32 MB	256-bit	256k x 32 x 4	4	1
1M x 32	16	64 MB	256-bit	256k x 32 x 4	4	2
2M x 32	2	16 MB	64-bit	512k x 32 x 4	1	1
2M x 32	4	32 MB	64-bit	512k x 32 x 4	1	2
2M x 32	4	32 MB	128-bit	512k x 32 x 4	2	1
2M x 32	8	64 MB	128-bit	512k x 32 x 4	2	2
2M x 32	8	64 MB	256-bit	512k x 32 x 4	4	1
2M x 32	16	128 MB	256-bit	512k x 32 x 4	4	2
4M x 32	2	32 MB	64-bit	1M x 32 x 4	1	1
4M x 32	4	64 MB	64-bit	1M x 32 x 4	1	2
4M x 32	4	64 MB	128-bit	1M x 32 x 4	2	1
4M x 32	8	128 MB	128-bit	1M x 32 x 4	2	2
4M x 32	8	128 MB	256-bit	1M x 32 x 4	4	1
4M x 32	16	256 MB	256-bit	1M x 32 x 4	4	2
4M x 16	4	32 MB	64-bit	1M x 16 x 4	1	1
4M x 16	8	64 MB	64-bit	1M x 16 x 4	1	2
4M x 16	8	64 MB	128-bit	1M x 16 x 4	2	1
4M x 16	16	128 MB	256-bit	1M x 16 x 4	4	1
8M x 32	2	64 MB	64-bit	2M x 32 x 4	1	1
8M x 32	4	128 MB	64-bit	2M x 32 x 4	1	2
8M x 32	4	128 MB	128-bit	2M x 32 x 4	2	1
8M x 32	8	256 MB	256-bit	2M x 32 x 4	4	1
8M x 16	4	64 MB	64-bit	2M x 16 x 4	1	1
8M x 16	8	128 MB	64-bit	2M x 16 x 4	1	2
8M x 16	8	128 MB	128-bit	2M x 16 x 4	2	1
8M x 16	16	256 MB	256-bit	2M x 16 x 4	4	1
16M x 16	4	128 MB	64-bit	4M x 16 x 4	1	1
16M x 16	8	256 MB	128-bit	4M x 16 x 4	2	1

3.10.2 Memory Address Mapping:

A[31:0] = input byte address

Table 3-2 Mapping between Address and Channel/Bank/Column/Page

	Address		
Channel/Bank/Column/Page	**4 Channel System**	**2 Channel System**	**1 Channel System**
Channel	A[8:7]	A[7]	--
Bank[1:0]	A[10:9]	A[10:9]	A[10:9]
Column[7:2] (prefetch of 4) 256 columns	A[14:11], A[6:5]	A[13:11], A[7:5]	A[12:11], A[8:5]
Column[8:2] (prefetch of 4) 512 columns	A[15:11], A[6:5]	A[14:11], A[7:5]	A[13:11], A[8:5]
Row[12:0] for 256 columns	A[27:15]	A[26:14]	A[25:13]
Row[12:0] for 512 columns	A[28:16]	A[27:15]	A[26:14]

Note: When the 2K mode is set, A[12:11] is used instead of A[8:7] as the channel select. In this case, A[8:7] will be used as the column bits.

3.11 BIOS ROM (Flash ROM) Interface

Due to timing and electrical restrictions on most IO pins of the chip, a very limited number of pins is available for the implementation of straps. In order to provide the initialization information to the chip, some of the straps are implemented as pull-ups and pull-downs on the video port pins. The remaining straps are stored inside the BIOS ROM and read during reset.

Five types of EPROM or Flash ROM are supported:

- Standard parallel EPROM or Flash ROM with external latches
- ATMEL Serial Flash ROM, AT25F1024 N-10SC-2.7
- ATMEL Serial Flash ROM, AT45DB011-SC
- ST Microelectronics Serial Flash ROM M25P10-VMN6 (1M) or M25P05-VMN6 (512K)
- NexFlash Serial Flash ROM NX25F011B-3S1 (1M), or NX25F015B-3S1 (512K)

3.11.1 Standard Boot-up Sequence

7. PCI reset is asserted.
8. External straps are fed into the chip.
9. PCI reset is deasserted and external straps are latched in.
10. ROM state machine begins to read “ROM based straps”. Note that this operation occurs only in the add-in card implementation.
11. PCI may begin its first transfer, taken but not serviced yet.
12. Finished reading the straps and begin processing PCI request.
13. Setup of PCI configuration space during system BIOS bus emulation.
14. Copy ROM into system memory.

There are three configurations for strap/BIOS implementation:

Configuration 1. The controller is located on an add-in card, and there is access to a local video BIOS EPROM / Flash RAM.

The sequence of events at power up is as follows:

1. System reset goes active and the strap latches are opened to read pin level straps.
2. Reset is removed, thereby closing the pin based strap latches.
3. A local routine between the controller and the eprom is initiated to read the additional straps stored in the eprom.

4. The first PCI configuration cycle is initiated and the eprom is read and stored in the system memory.
5. Standard operations can begin.

The ROM state machine of the RADEON 9800 will read in all the “ROM based straps” right after PCI reset is deasserted. There are a total of 10 bytes worth of “ROM based straps” which are stored at byte location 0x70 through 0x79 in the eprom/flashrom. See *Table 3-17, “ROM Based Straps,” on page 16* for details.

Configuration 2. The controller is located on the system motherboard and the video BIOS is stored in the system BIOS EPROM/Flash RAM.

The sequence of events at power up is as follows:

1. System reset goes active and the strap latches are opened to read pin level straps.
2. Reset is removed, thereby closing the pin based strap latches.
3. The first PCI config cycle is initiated and the additional straps stored in the system BIOS are written into the controller. This occurs before POST begins in system BIOS, as per OS requirements.
4. Standard operations can begin.

The System BIOS will be responsible for loading the SUBSYSTEM_ID and SUBSYSTEM_VENDOR_ID through an aliased address in the controller chip's reserved configuration space. The reason for writing through an aliased address (0x14C) is that the config location 0x12C is read only. Any writes to this location (0x14C) will also change the content of the SUBSYSTEM_VENDOR_ID at 0x12C. Since there is no ROM, the functionality of the CHG_ID ROM based strap will be carried out by the ROMIDCFG pin straps.

Configuration 3. Combination of configurations **1** and **2** (add-in card and device on motherboard)

The system BIOS will take care of the graphics device on the motherboard as in case 2, while the chip on the add-in board will be taken care of as in case 1. This should cover the situation where the OS does not read the add-in card’s video BIOS because the ROM state machine from the graphics chip reads the “ROM based straps” independently from the video BIOS.

Note: If neither the system BIOS nor the add-in card video BIOS supply the SUBSYSTEM_ID and SUBSYSTEM_VENDOR_ID, their values are defaulted to CHIP_ID and VENDOR_ID (1002h) respectively inside the chip.

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Chapter 4
Signal Description and Strap Options

This chapter gives the signal descriptions of the RADEON 9800 pins and strap options. All active low signals are shown with the suffix ‘b’ (e.g., RSTb).

To jump to a topic of interest, use the following list of hypertext linked cross references:

4.1 Signal Description

4.1.1 Host PCI/AGP

Table 4-1 Host PCI/AGP

Signal Name	Type	Functional Description
RSTb	I	Active Low PCI Reset, All PCI signals on the RADEON 9800 will be tri-stated during its assertion This signal may be asserted or de-asserted asynchronously to the PCICLK, but it must be guaranteed to be clean and have bounce-free edges.
PCICLK	I	Bus Clock, this signal is used as a reference for all transactions on the PCI bus. Except for RSTb and INTAb, all PCI signals are sampled on the rising edge of this clock signal and all timing parameters are defined with respect to this rising edge. It's frequency can be 33 - 66 Mhz depending on the system bus type (PCI 33 - PCI 66 – AGP)
AD(31:0)	I/O	Address/Data (31:0) A bus cycle consists of an address phase followed by one or more data phases. **PCI:** when the RADEON 9800 is a target on the PCI bus, these signals are inputs for address read/writes and write data, and outputs for read data. This bus contains the address during the clock cycle in which FRAMEb is asserted (address phase), and it contains the data in the subsequent clock cycles. **AGP:** the RADEON 9800 acts as an AGP master. Data is driven or received through the AD lines by the RADEON 9800 after appropriate commands are sent to the host-to-PCI bridge via the side band address bus (SBA(7:0)) Note: in AGP mode, AD16 or AD17 (depending on the IDSELb strap setting) are also used for the IDSEL function.
C_BEb(3:0)	I/O	Bus Command/ Byte Enable(3:0) **PCI:** during the address phase of a transaction, these signals define the bus command (Int ack., spec. cycle, IO R/W, Mem R/W, Config R/W, etc.). During the data phase, they are used as Byte Enables (determine which byte on the AD line carries meaningful data) **AGP:** provide valid byte information during AGP write transactions and are driven by the master. They are driven to '0000' by the target and ignored by the master (RADEON 9800) during the return of AGP read data.
FRAMEb	I/O	Cycle Frame **PCI:** this signal is driven by the current master to indicate the beginning and duration of an access. It is asserted to indicate the beginning of a bus transaction. Data transfer will continue while this signal is asserted. When FRAMEb is deasserted, the transaction is in its final data phase. **AGP:** not used in AGP and kept in its deasserted state
IRDYb	I/O	Initiator (bus master) ready **PCI:** it indicates the ability of the current initiator (current bus master) to complete the current data phase of the transaction. During a write cycle, IRDYb indicates that valid data is present on the AD line. During a read cycle, it indicates that the master is ready to accept data. IRDYb is used in conjunction with the TRDYb signal. Wait cycles are inserted until both IRDYb and TRDYb are asserted. A data phase is completed on any clock where both IRDYb and TRDYb are sampled as asserted. **AGP:** for AGP writes, it indicates that the master is ready to provide all write data for the current write transaction. Once this signal is asserted for a write operation, the master is not allowed to insert wait states. For AGP reads, the assertion of this signal indicates that the master is ready to accept a subsequent block (32 bytes) of read data. the master is never allowed to insert a wait state during the initial block of a read transaction, but it may do so after subsequent block transfers. (there is no FRAMEb -- IRDYb relationship for AGP transactions) The target is allowed to insert wait states on block boundaries but not on individual data phases (for both Read and Write operations)
TRDYb	I/O	Target device ready **PCI:** it indicates the ability of the target to complete the current data phase of the transaction During a read cycle, TRDYb indicate that valid data is present on the AD line. During a write cycle, it indicates that the target is ready to accept data. TRDYb is used in conjunction with IRDYb. Wait cycles are inserted until both IRDYb and TRDYb are asserted. A data phase is completed on any clock where both IRDYb and TRDYb are sampled as asserted. **AGP:** for AGP reads, it indicates that the target is ready to provide read data for the entire transaction (when transaction can complete within four clocks) or is ready to transfer a (initial or subsequent) block of data when the transfer requires more than four clocks to complete. The target is allowed to insert wait states after each block transfers on both read and write transaction

Table 4-1 Host PCI/AGP (Continued)

Signal Name	Type	Functional Description
DEVSELb	I/O	Device select **PCI:** when actively driven, it indicates that the driving device (target) has decoded its address as the target of the current access. As an input to other devices and the current master, it indicates whether any device on the bus has been selected. **AGP:** not used in AGP and kept in its deasserted state
STOPb	I/O	Target transaction termination request **PCI:** it indicates that the current target is requesting the master to stop the current transaction **AGP:** not used in AGP and kept in its deasserted state
PAR	O	Parity bit for AD(31:0) and C/BEb(3:0) **PCI:** parity is even across the AD and C/BEb lines. It means that PAR = 1 when the count of the number of '1s' on the AD, C/BEb and PAR line is even. Parity generation is required by all PCI agents. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDYb is asserted on a write transaction or TRDYb is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. PAR has the same timing as the AD line but delayed by one clock. The master drives PAR for address and write data phases and the target drives PAR for read data phases. **AGP:** not used in AGP but must be actively driven by the current owner of the AD bus
INTAb	O	Interrupt request line **PCI and AGP:** used to request an interrupt. It's a shareable, level sensitive, active low signal. INTAb is for a single function device
REQb	I/O	PCI Bus Master Request signal to arbiter **PCI and AGP:** this signal indicates to the arbiter that this agent desires the use of the bus. This is a point to point signal (i.e. each master has its own REQb line)
GNTb	I	PCI Bus Master Grant signal from arbiter **PCI:** this signal indicates to the agent that access to the bus has been granted by the arbiter. This is a point to point signal (i.e. each master has its own REQb line) **AGP:** same as PCI but used in combination with the ST signals. the additional information provided by the ST lines indicates whether the master is the recipient of previously requested read data (high or low priority), or whether it is to provide write data (high or low priority) for a previously enqueued write command, or whether it has been given permission to start a bus transaction (AGP or PCI)
ST(2:0)	I	AGP Status bus **AGP:** these signals provide information from the arbiter to the master on what it may do. The ST lines have meaning to the master only when that master's GNTb is asserted. When GNTb is not asserted, these signals have no meaning and must be ignored
SBA(7)	I/O	AGP Sideband Address port bit 7 **or** PCI Initialization device select (IDSEL in PCI mode) **PCI:** it is used as a chip select during configuration read and write cycles **AGP:** AGP sideband address port bit 7
SBA(6:0)	O	Sideband Address port for AGP1X/2X/4X/8X support **AGP:** it's an additional bus used to pass requests (address and command) to the target from the master. Note: No ATI AGP device uses the PIPEb mechanism to enqueue requests. It uses the SBA lines to enqueue requests to the arbiter.
RBFb	O	AGP Read buffer full **AGP:** this signal indicates whether the master is ready to accept previously requested low priority read data or not. When asserted, the arbiter is not allowed to initiate the return of low priority read data to the master.
AD_STBF(1:0)	I/O	AGP Address strobe **AGP:** AD_STB0 and AD_STB1 provide timing for AGP2x,4x,8x data transfer mode on respectively AD(15:0) and AD(31:16). The agent that is providing data drives this signal.
SB_STBF	I/O	Sideband Strobe for AGP1X/2X/4X/8X support **AGP:** this signal provides timing for the SBA lines (when supported) and is always driven by the master. When the side band strobe has been idle, a sync. cycle need to be performed before a request can be enqueued.
AD_STBS(1:0)	I/O	AGP Address strobe differential complement **AGP:** differential complement of AD_STBF(1:0)
SB_STBS	I/O	Sideband Strobe differential complement **AGP:** differential complement of SB_STBF

Table 4-1 Host PCI/AGP (Continued)

Signal Name	Type	Functional Description
AGPTEST	A-O	Analog Output AGPTest provides a fixed reference, through a resistor to VDDP, for the internal compensation of signal strength. The compensator will drive the resistor with an output buffer in the AGPTEST pad, and measure the voltage. This voltage is an indication of the strength of the output driver. The compensator will adjust strengths accordingly. 3.3V bus signaling (PCI or AGP): unused, leave pin unconnected. AGP 2.0 mode :resistor value should be 50 ohm +/-1% AGP 3.0 mode :resistor value should be 169 ohm +/-1% (Both AGP 2.0 and 3.0 modes can be supported using a circuit which adds a 71.5 Ohm resistor in parallel with the 169Ohm resistor when AGP 3.0 mode is not detected.)
AGPREF	A-I	Analog Input Reference Voltage for differential receivers 3.3V bus signaling (PCI or AGP): unused, should be set to 1.8V AGP 2.0 mode :VDDP / 2 AGP 3.0 mode : 0.233* VDDP (0.35V)
DBI_HI	I/O	Data Bus Invert High This is a source synchronous bit that goes along with AD[31:16] to indicate whether AD[31:16] needs to be inverted on the receiving end. DBI_HI = 0 AD[31:16] is not inverted so receiver may use as is DBI_HI = 1 AD[31:16] is inverted so receiver must invert before use.
DBI_LO	I/O	Data Bus Invert Low This is a source synchronous bit that goes along with AD[15:00] to indicate whether AD[15:00] needs to be inverted on the receiving end. DBI_LO = 0 AD[15:00] is not inverted so receiver may use as is DBI_LO = 1 AD[15:00] is inverted so receiver must invert before use.
WBFb	O	AGP: this signal indicates that the fast write buffer is full. If asserted, the fast write master is not allowed to send fast write data.
AGP8X_DETb	I	AGP 8X signalling detect: 0: Motherboard and GC both 8x capable 1: Either Motherboard or GC not 8x capable Notes: AGP8X_DETb is either connected directly to MB_AGP8X_DET# (on AGP connector) or made open via a 0 ohm resistor. The resistor is removed if we wish to enforce 1.5V signaling. Also note that **if this 0 ohm resistor is removed, so to must the 0 ohm resistor connecting GC_AGP8X_DET# to ground**. This pin should be pulled up internally

4.1.2 Memory A SDRAM

Table 4-2 Memory A SDRAM

Signal Name	Type	Functional Descriptions
DQA(63:0)	I/O	Memory Data Bus Channel A Supports SSTL2 and SSTL3 (DDR)
DQMAb(7:0)	I/O	Byte enables / Byte invert Memory data byte enables for write cycles.
DIMA(1:0)	O	Data Inversion Mask
MAA(13:0)	O	Memory Address Bus Provide multiplexed row and column addresses to the S(D/G)RAMs. MAA(13) is always BA(1). MAA(12) is BA(0) for 4 bank S(D/G)RAMs.
MAA(14)	O	Memory Address Bus bit 14 Provide multiplexed row and column address to the S(D/G)RAMs. For single rank of 256M SDRAM, row address 12. For 2 rank configuration., used as second chip select -CSAb(1).
CSAb(0)	O	Chip select Chip select for SDRAM (for first rank when in two rank configuration.)
QSA(7:0)	I/O	DDR data strobes, these strobes are used to latch data into the chip and the DDR S(D/G)RAMs.
RASAb	O	Row Address Strobe
CASAb	O	Column Address Strobe
WEAb	O	Write enable

Table 4-2 Memory A SDRAM (Continued)

Signal Name	Type	Functional Descriptions
CKEA	O	Clock enable control
CLKA0	I/O	Memory clock 0
CLKA0b	I/O	Memory clock 0 bar
CLKA1	I/O	Memory clock 1
CLKA1b	I/O	Memory clock 1 bar
VREF(1:0)	A-I	Reference voltage (1.25V Typ. for SSTL-2 / 0.5 * VDD) (1.5V Typ. for SSTL-3 / 0.45 * VDD) Connect to VDDR1/2 except when VDDR1=3.3V, in which case, connect to 1.8V through 100K resistor. Note: if the differential signaling interface is not used, this pin must be connected to 1.8V through 100K resistor.

4.1.3 Memory B SDRAM

Table 4-3 Memory B SDRAM

Signal Name	Type	Functional Descriptions
DQB(63:0)	I/O	Memory Data Bus Supports SSTL2 and SSTL3 (DDR)
DQMBb(7:0)	I/O	Byte enables / Byte invert Memory data byte enables for write cycles.
DIMB(1:0)	O	Data Inversion Mask
MAB(13:0)	O	Memory Address Bus Provide multiplexed row and column addresses to the S(D/G)RAMs. MAB(13) is always BA(1). MAB(12) is BA(0) for 4 bank S(D/G)RAMs.
MAB(14)	O	Memory Address Bus bit 14 Provide multiplexed row and column address to the S(D/G)RAMs. For single rank of 256M SDRAM, row address 12. For 2 rank configuration., used as second chip select -CSBb(1).
CSBb(0)	O	Chip select Chip select for SDRAM (for first rank when in two rank configuration.)
QSB(7:0)	I/O	DDR data strobes, these strobes are used to latch data into the chip and the DDR S(D/G)RAMs.
RASBb	O	Row Address Strobe
CASBb	O	Column Address Strobe
WEBb	O	Write enable
CKEB	O	Clock enable control
CLKB0	I/O	Memory clock 0
CLKB0b	I/O	Memory clock 0 bar
CLKB1	I/O	Memory clock 1
CLKB1b	I/O	Memory clock 1 bar

4.1.4 Memory C SDRAM

Table 4-4 Memory C SDRAM

Signal Name	Type	Functional Description
DQC(63:0)	I/O	Memory Data Bus Supports SSTL2 and SSTL3 (DDR)
DQMCb(7:0)	I/O	Byte enables / Byte invert Memory data byte enables for write cycles.
DIMC(1:0)	O	Data Inversion Mask
MAC(13:0)	O	Memory Address Bus Provide multiplexed row and column addresses to the S(D/G)RAMs. MAC(13) is always BA(1). MAC(12) is BA(0) for 4 bank S(D/G)RAMs.

Table 4-4 Memory C SDRAM

Signal Name	Type	Functional Description
MAC(14)	O	Memory Address Bus bit 14 Provide multiplexed row and column address to the S(D/G)RAMs. For single rank of 256M SDRAM, row address 12. For 2 rank configuration., used as second chip select -CSCb(1).
CSCb(0)	O	Chip select Chip select for SDRAM (for first rank when in two rank configuration.)
QSC(7:0)	I/O	DDR data strobes, these strobes are used to latch data into the chip and the DDR S(D/G)RAMs.
RASCb	O	Row Address Strobe
CASCb	O	Column Address Strobe
WECb	O	Write enable
CKEC	O	Clock enable control
CLKC0	I/O	Memory clock 0
CLKC0b	I/O	Memory clock 0 bar
CLKC1	I/O	Memory clock 1
CLKC1b	I/O	Memory clock 1 bar

4.1.5 Memory D SDRAM

Table 4-5 Memory D SDRAM

Signal Name	Type	Functional Descriptions
DQD(63:0)	I/O	Memory Data Bus Supports SSTL2 and SSTL3 (DDR)
DQMDb(7:0)	I/O	Byte enables / Byte invert Memory data byte enables for write cycles.
DIMD(1:0)	O	Data Inversion Mask
MAD (13:0)	O	Memory Address Bus Provide multiplexed row and column addresses to the S(D/G)RAMs. MAD(13) is always BA(1). MAD(12) is BA(0) for 4 bank S(D/G)RAMs.
MAD(14)	O	Memory Address Bus bit 14 Provide multiplexed row and column address to the S(D/G)RAMs. For single rank of 256M SDRAM, row address 12. For 2 rank configuration., used as second chip select -CSDb(1).
CSDb(0)	O	Chip select Chip select for SDRAM (for first rank when in two rank configuration.)
QSD(7:0)	I/O	DDR data strobes, these strobes are used to latch data into the chip and the DDR S(D/G)RAMs.
RASDb	O	Row Address Strobe
CASDb	O	Column Address Strobe
WEDb	O	Write enable
CKED	O	Clock enable control
CLKD0	I/O	Memory clock 0
CLKD0b	I/O	Memory clock 0 bar
CLKD1	I/O	Memory clock 1
CLKD1b	I/O	Memory clock 1 bar
MEMTEST	A-O	This pin is used to control the variable drive capability of the memory section I/Os. It is connected to ground through a 45 ohm resistor. The P transistors of the output buffer in the MEMTEST I/O will drive a current through this resistor and the resultant voltage is used to measure and calibrate the drive capability.
MEMVMODE(1:0)	I/O	Voltage value for S(D/G)RAM chips: “01” for VDDR1 2.5V (DDR) “10” for VDDR1 1.8V (DDR) *** Note: these pins must be connected on the PCB; there is no default value. A logical “1” on these pins is considered to be 1.8V. A logical “0” is considered to be ground potential.

4.1.6 Integrated TMDS

Note: TMDS data/clock channels transmit at a bit rate of 10x pixel clock, up to 165MHz pixel clock (when the TMDS coherency setting matches the receiver coherency mode; otherwise, 135MHz).

Table 4-6 Integrated TMDS

Signal Name	Type	Functional Descriptions
TX0P	A-O	TMDS data channel 0 (+) Care should be taken to route each differential signal pair together and minimize the number of vias the signal lines are routed through. Do not split the pairs and minimize the number of vias. Vias are very inductive and can cause phase delay problems if applied unevenly with a pair.
TX0M	A-O	TMDS data channel 0 (-) Guideline same as TX0P
TX1P	A-O	TMDS data channel 1 (+) Guideline same as TX0P
TX1M	A-O	TMDS data channel 1 (-) Guideline same as TX0P
TX2P	A-O	TMDS data channel 2 (+) Guideline same as TX0P
TX2M	A-O	TMDS data channel 2 (-) Guideline same as TX0P
TXCP	A-O	TMDS clock channel (+) Guideline same as TX0P
TXCM	A-O	TMDS clock channel (-) Guideline same as TX0P
TPVDD	I	Powering TMDS PLL macro **(1.8V)** Keep the power supply clean TPVDD should have its own voltage regulator on board.The regulator helps filter out voltage fluctuations. Voltage fluctuations may cause reduced operating range or performance problems due to noise-induced jitter to the TMDS PLL. TPVDD trace on board should be routed directly from the ball for TPVDD and tapped off with one via at the TPVDD on the regulator Decoupling capacitors is recommended on TPVDD if the power plane is very noise
TPVSS	O	TMDS PLL macro ground pin Keep the ground clean. TPVSS should have its own voltage regulator on board. TPVSS trace on board should be routed directly from the ball for TPVSS and tapped off with one via at the TPVSS on the regulator
TXVDDR(x2)	I	Power TMDS IOs. **(1.8V)** TXVDDR should have its own voltage regulator on board TXVDDR trace on board should be routed directly from the ball for TXVDDR and tapped off with one via at the TXVDDR on the regulator.
TXVSSR(x3)	O	TMDS IO ground pins TXVSSR should have its own voltage regulator on board TXVSSR trace on board should be routed directly from the ball for TXVSSR and tapped off with one via at the TXVSSR on the regulator.

4.1.7 VIP Capture

Table 4-7 VIP Capture

Signal Name	Type	Functional Description
VID(7)	I/O	VIP video capture port data(7); TMS, IEEE 1149.1 test mode select
VID(6)	I/O	VIP video capture port data(6); TCK, IEEE 1149.1 clock
VID(5)	I/O	VIP video capture port data(5); TDI, IEEE 1149.1 data in
VID(4)	I/O	VIP video capture port data(4); TDO, IEEE 1149.1 data out
VID(3)	I/O	IEEE jtag interface TRST signal
VID(2)	I/O	Scan shift enable pin

Table 4-7 VIP Capture (Continued)

Signal Name	Type	Functional Description
VID(1)	I/O	Clock-gating disable pin for scan mode
VID(0)	I/O	Scan mode pin
DVALID	I/O	Scan input/output pin permission signal
PSYNC	I/O	Transport stream sync input. GPIO if transport stream capture not used.
VPCLK0	I/O	VIP video capture port clock

4.1.8 VIP Host

Table 4-8 VIP Host

Signal Name	Type	Functional Description
VHAD(1)	I/O	VIP host port address/data bit 1.
VHAD(0)	I/O	VIP host port address/data bit 0. VIP_DEVICE strap to indicate if any slave VIP host devices attached.
VPHCTL	I/O	VIP host port control signal.
VIPCLK	I/O	VIP host port clock.

4.1.9 MMI2C

Table 4-9 VIP Host

Signal Name	Type	Functional Description
SCL	I/0	I^2C clock
SDA	I/0	I^2C data

4.1.10 DVO

Table 4-10 DVO

Signal Name	Type	Functional Description
DVOCLK(1:0)	O	Differential clock outputs for DDR DVO/TVO data output. Or DVOCLK(0) is used by itself for single ended clocking or for SDR mode.
DVOCNTL(2:0)	I/O	DVOCNTL(0) -- Data Enable DVOCNTL(1) – HSYNC DVOCNTL(2) – VSYNC
DVODATA(11:0)	I/O	DVO data output bus.
DVOVMODE	I	DVO pads voltage select for DVOCLK(1:0), DVOCNTL(2:0) and DVODATA(11:0). When DDR, VDDR4=1.8V and DVOVMODE=1.8V When SDR, VDDR4=3.3V and DVOVMODE=0V

4.1.11 TVO

Table 4-11 TVO

Signal Name	Type	Functional Description
TVOCLKI	I/O	Clock from external video encoder to graphics controller. DVO data bit 23 when used as part of 24 bit DVO port.
TVOCLKO	I/O	Clock from graphics controller to external video encoder. DVO data bit 22 when used as part of 24 bit DVO port.

Table 4-11 TVO (Continued)

Signal Name	Type	Functional Description
TVODATA(9:0)	I/O	Data bus to external video encoder such as ATI Rage Theater or ITU-656 compatible encoder. Use TVODATA(9:2) to connect to 8 bit encoders. DVO data bits 21:12 when used as part of 24 bit DVO port. TVODATA(0) also optional external trigger input signal to synchronize 2D/3D rendering engines with external events.
TVOVMODE	I	TVO pads voltage select for TVODATA, TVOCLKI, TVOVLKO. For SDR DVO or dual channel DVO must be same as DVOVMODE. For TVO or ROM must be 0V. When DDR DVO, VDDR2=1.8V and TVOVMODE=1.8V When TVO, ROM or SDR DVO, VDDR2=3.3V and TVOVMODE=0V

4.1.12 DAC (CRT)

Table 4-12 DAC (CRT)

Signal Name	Type	Functional Description
R	A-O	Red for monitor Analog DAC output, designed to drive a 37.5 Ohm equivalent load, driving the Red pin of the monitor (37.5 Ohm = 75 Ohm pull-down resistor on board in parallel with the 75 Ohm CRT load/Impedance). The board traces for R, G, B outputs of both DACs should have 75ohms characteristic impedance
G	A-O	Green for monitor Analog DAC output, designed to drive a 37.5 Ohm equivalent load, driving the Green pin of the monitor (37.5 Ohm = 75 Ohm pull-down resistor on board in parallel with the 75 Ohm CRT load/Impedance). The board traces for R, G, B outputs of both DACs should have 75ohms characteristic impedance
B	A-O	Blue for monitor Analog DAC output, designed to drive a 37.5 Ohm equivalent load, driving the Blue pin of the monitor (37.5 Ohm = 75 Ohm pull-down resistor on board in parallel with the 75 Ohm CRT load/Impedance). The board traces for R, G, B outputs of both DACs should have 75ohms characteristic impedance
HSYNC	I/O	Horizontal sync for Monitor This signal requires an on board TTL buffer (for e.g. LS125)
VSYNC	I/O	Vertical sync for Monitor This signal requires an on board TTL buffer (for e.g. LS125)
STEREOSYNC	I/O	Stereo display sync signal. Indicates left/right frame, or top/bottom field
AUXWIN	I/O	**Dual functionality**: Special output pin for Apple or Geyserville interrupt pin for 'Wintel' platforms
AVDD	I	DAC VDD **(1.8V)** Dedicated power for CRT DAC. Effort should be made at the board level to provide as clean a power as possible to this pin to avoid noise injection in the DAC which in term can affect the display quality. Adequate decoupling should be provided between this pin and AVSSN.
AVSSN	O	DAC VSS. Noisy current dump for DAC. Dedicated ground for CRT DAC. Effort should be made at the board level to provide as clean a ground as possible to this pin to avoid noise injection in the DAC which in term can affect the display quality. Pay special attention to keep inductance on this ground node to as small as possible Adequate decoupling should be provided between this pin and AVDD.
VDD1DI	I	Digital **1.8V** supply for the logic portion of the DAC
VSS1DI	I	Corresponding digital ground for VDD1DI
AVSSQ	Gnd	Band Gap Ref. VSS Dedicated ground for the CRT Band Gap Reference (DAC). Effort should be made at the board level to provide as clean a ground as possible to this pin to avoid noise injection in the DAC which in term can affect the display quality. Adequate decoupling should be provided between this pin and AVDD.
RSET	O	Internal DAC reference Used to set the full scale DAC current through a high precision resistor (1%) of 499 Ohm (preliminary value) placed between this pin and AVSSQ.

4.1.13 DAC2 (TV/CRT2)

Table 4-13 DAC2 (TV/CRT2)

Signal Name	Type	Functional Description
Y_G	A-O	SVID Y output for TV out, **Or** Green for 2nd CRT Monitor Or luminance for component video YPbPr TV out Again expected to drive a equivalent 37.5 ohm load. The board traces for R, G, B outputs of both DACs should have 75ohms characteristic impedance
C_R	A-O	SVID C output for TV out, **Or** Red for 2nd CRT Monitor Or Pr for component video YPbPr TV out Again expected to drive a equivalent 37.5 ohm load. The board traces for R, G, B outputs of both DACs should have 75ohms characteristic impedance
COMP_B	A-O	Composite Video for TV out, **Or** Blue for 2nd CRT Monitor Or Pb for component video YPbPr TV out Again expected to drive a equivalent 37.5 ohm load. The board traces for R, G, B outputs of both DACs should have 75ohms characteristic impedance
H2SYNC	I/O	Horizontal Sync for 2nd CRT when TV out is not used.
V2SYNC	I/O	Vertical Sync for 2nd CRT when TV out is not used.
A2VDD	I	DAC2 VDD **(2.5V)** Dedicated power for TV DAC. Effort should be made at the board level to provide as clean a power as possible to this pin to avoid noise injection in the DAC which in term can affect the display quality. Adequate decoupling should be provided between this pin and A2VSSN.
VDD2DI	I	Digital **1.8V** supply for the logic portion of TVDAC
VSS2DI	I	Corresponding digital ground for VDD2DI
A2VDDQ	Pwr	DAC2 Band Gap Ref. Voltage **(1.8V)** Dedicated power for TV DAC. Effort should be made at the board level to provide as clean a power as possible to this pin to avoid noise injection in the DAC which in term can affect the display quality. Adequate decoupling should be provided between this pin and AVSSQ.
A2VSSQ	Gnd	DAC2 VSS (quiet ground; use for Band Gap) Should never be tied to noisy CORE ground, nor to A2VSSN. Adequate decoupling should be provided between this pin and A2VDDQ.
A2VSSN	Gnd	DAC2 VSS (noisy ground; used as current dump) Effort should be made to minimize the inductance at this node. Adequate decoupling should be provided between this pin and A2VDD.
R2SET	O	Internal Reference for second DAC Used to set the full scale DAC current through a high precision resistor (1%) of 715 Ohm (preliminary value) placed between this pin and A2VSSQ.

4.1.14 Monitor Interface

Table 4-14 Monitor Interface

Signal Name	Type	Functional Description
DDC1DATA	I/O	Primary connector DDC data pin. Should be used for primary VGA connector, may also be for second TMDS.
DDC1CLK	I/O	Primary connector DDC clock pin
DDC2DATA	I/O	Secondary connector DDC data. Should be used for primary TMDS connector. Supports HDCP. May also be used for secondary VGA connector.
DDC2CLK	I/O	DDC pin used for Panel ID; SCL functionality for TMDS
HPD1	I	Primary hot plug detect. Not used if primary connector non-DVI.
HPD2	I	Secondary hot plug detect. Not used if secondary connector non-DVI.

4.1.15 Test Pins

Table 4-15 Test Pins

Signal Name	Type	Functional Description
TESTEN	I	Test mode enable (Other 4 signals are muxed on VID); must be connected to ground for normal operation. It is also used as TRSTb pin
TEST_AGPCLK	I	Input test clock for AGPCLK
TEST_YCLK	I	Input test clock for YCLK (2x mem)
TEST_MCLK	I	Input test clock for MCLK (1x mem)

4.1.16 ROM Interface

Table 4-16 ROM Interface

Signal Name	Type	Functional Description
ROMCSb	I/O	BIOS ROM Chip Select Used to enable the Rom for Rom Read and Write (if flashrom) operations.
ROMSI	I/O	BIOS ROM Serial Input Serial data input to ROM (output of Khan)
ROMSO	I/O	BIOS ROM Serial Output Serial data output from ROM (input to Khan)
ROMSCK	I/O	BIOS ROM Serial Clock Clock for serial input / output data streams

4.1.17 PLLs & XTAL Interface

Table 4-17 PLLs & XTAL

Signal Name	Type	Functional Description
XTALIN	I	PLL Reference Clock or MXCLK source (14.318 - 29.4989 Mhz) (1.5V Input level)
XTALOUT	I/O	PLL Reference Clock (1.5V Input level) A series resonant crystal can be connected between these two pins to provide the reference clock for the internal PLLs of RADEON 9800. An external LVTTL (1.5V) Oscillator can also be connected to XTALIN or XTALOUT to provide the reference clock. In order to provide reliable functionality, proper video synchronization and high quality display, it is recommended that the crystal/oscillator should have as small an error (50 ppm) and jitter as possible, with a balanced duty cycle (55-45 worst case). Xtal characteristics (also valid for Oscillators): -Frequency: 27.000 Mhz (if with TVout) -Accuracy: 50 ppm -Duty cycle (worst case): 45-55 (max) -Jitter: 500 ps (max) cycle to cycle -Voltage supply: 2.5V / 3.3V with external resistor divider to bring XTALIN signal to 1.5V level.
PVDD	I	Phase Lock Loop Power **(1.8V)** Dedicated power pin for RADEON 9800 PLL's. Effort should be made at the board level to provide as clean a power as possible to this pin to avoid noise injection in the PLL's which in term can affect the display quality and functional reliability of the RADEON 9800. Adequate decoupling should be provided between this pin and PVSS. PVDD and PVSS should have their own regulator on board PVDD trace on board should be routed directly from the ball for PVDD and tapped off with one via at the PVDD on the regulator

Table 4-17 PLLs & XTAL (Continued)

Signal Name	Type	Functional Description
PVSS	O	Phase Lock Loop Ground Dedicated ground for the RADEON 9800 PLL's. Effort should be made at the board level to provide as clean a ground as possible to this pin to avoid noise injection in the PLL's which in term can affect the display quality and functional reliability of the RADEON 9800. adequate decoupling should be provided between this pin and PVDD. PVDD and PVSS should have their own regulator on board PVSS trace on board should be routed directly from the ball for PVSS and tapped off with one via at the PVSS on the regulator
MPVDD	I	Memory Phase Lock Loop Power **(1.8V)** Dedicated power pin for the RADEON 9800 memory PLL. Effort should be made at the board level to provide as clean a power as possible to this pin to avoid noise injection in the PLL's which in term can affect the display quality and functional reliability of the RADEON 9800. adequate decoupling should be provided between this pin and MPVSS. MPVDD and MPVSS should have their own regulator on board. MPVDD trace on board should be routed directly from the ball for MPVDD and tapped off with one via at the MPVDD on the regulator
MPVSS	O	Memory Phase Lock Loop Ground Dedicated ground for the RADEON 9800 Memory PLL. Effort should be made at the board level to provide as clean a ground as possible to this pin to avoid noise injection in the PLL's which in term can affect the display quality and functional reliability of the RADEON 9800. adequate decoupling should be provided between this pin and MPVDD. MPVDD and MPVSS should have their own regulator on board. MPVSS trace on board should be routed directly from the ball for MPVSS and tapped off with one via at the MPVSS on the regulator

4.1.18 Thermistor

Table 4-18 Thermistor

Signal Name	Type	Functional Description
VT1	O	Used for connecting to a fan management IC.
VT2	O	Used for connecting to a fan management IC.

4.1.19 Host Power

Table 4-19 Host Power

Signal Name	Type	Functional Description
VDDP	Pwr	**1.5V/3.3V** – PCI / AGP IO power for the AGP/PCI pins

4.1.20 IO Internal Power

Table 4-20 IO Internal Power

Signal Name	Type	Functional Description
VDDC18	Pwr	1.8V power for internal IO power

4.1.21 Memory IO Power

Table 4-21 Memory IO Power

Signal Name	Type	Functional Description
VDDR1 (memory)	Pwr	1.8V/2.5V (DDR) IO power for the memory bus.

4.1.22 Memory Clock Power

Table 4-22 Memory Clock Power

Signal Name	Type	Functional Description
VSSRH	Pwr	Dedicated ground pin for memory clock pads.
VDDRH	Pwr	1.8V/2.5V (DDR) Dedicated power pin for memory clock pads. It should have the same voltage level as VDDR1

4.1.23 IO Power

Table 4-23 IO Power

Signal Name	Type	Functional Description
VDDR3 (other digital)	Pwr	3.3V IO power for other pins

4.1.24 DVO Power

Table 4-24 DVO Power

Signal Name	Type	Functional Description
VDDR4	Pwr	1.8V/3.3V (DDR/SDR) Supply for DVOCLK(1:0), DVOCNTL(2:0), DVODATA(11:0)
VDDR2	Pwr	1.8V/3.3V (DDR/SDR) Supply for TVODATA(9:0), TVOCLKI, TVOCLKO

4.1.25 IO Ground

Table 4-25 IO Ground

Signal Name	Type	Functional Description
VSSP	Gnd	AGP IO VSS

4.1.26 Core Power

Table 4-26 Core Power

Signal Name	Type	Functional Description
VDDC	Pwr	**1.5V to 1.77V** dedicated core power, provides power to internal logic
VDDCI	Pwr	1.5V to 1.77V isolated core power, on the PCB same as VDDC

4.1.27 IO Core / Ground

Table 4-27 IO Core / Ground

Signal Name	Type	Functional Description
VSS	Gnd	Ground

4.2 Strap Options

The RADEON 9800 chips can work with either no ROM attached, or a small attached ROM that contains configuration information (but no video BIOS), or a large attached ROM that contains a video BIOS and configuration information.

When a ROM is attached, ROM based straps are read from the ROM after hardware reset and before host bus interface cycles from the system are accepted by the chip. This allows details of how the chip will declare itself to the system to be

set by the ROM based straps.

The full details of RADEON 9800 strapping options are outlined below.

Attached ROMs may optionally contain HDCP encryption keys. If the ROM does not contain these keys, then HDCP encryption can not be enabled. The ROM controller contains logic to disable writing to the section of the ROM containing HDCP keys after initial programming in production.

If a large ROM is attached, it will contain a PCI compliant video BIOS. Whether or not this BIOS is used depends on the system BIOS and the operating system.

The ROM controller supports PROM, EPROM and FlashROM type devices. FlashROM devices can be reprogrammed with a new video BIOS in a target system using an ATI supplied flash utility.

Large ROMs must be used on all add-in cards. These may be 64 kbyte or 128 kbyte in size. Both parallel and serial ROM types are supported. Parallel ROMs require external latching circuitry to multiplex the ROM address, data and control signals onto a small number of IO pins. Large serial ROMs of various SPI types are supported. The exact set of serial ROM types supported is listed in *Table 4-28, "Pin Based Straps," on page 4-14*.

Parallel ROM connection will be multiplexed on the TVODATA pins or on the DVODATA pins. If either the TVO port or the DVO port are used for other functions on a specific board (video encoder or TMDS encoder), then parallel ROM will not be an option on that port. If both ports are not available for parallel ROM on a board, then that board must use a serial ROM.

There are pin based straps to indicate the attached ROM type, or if no ROM is attached. In cases where no ROM is attached, there are default values used for all ROM based straps.

There are three types of straps in RADEON 9800:

- Bonding straps. These are listed above in the section *"Signal Description" on page 4-2*
- Pin based straps.
- ROM based straps.

The bonding straps and pin based straps must always be correctly configured. If a valid programmed ROM is attached, then the ROM based straps will also be read and used after hardware reset. If no ROM is attached, or the attached ROM is not programmed, then defaults will be used for these values.

4.2.1 Pin Based Straps

Table 4-28 Pin Based Straps

Strap	Pin	Functional Description	Default
id_disable	PSYNC	0- Normal operation 1- Shuts the chip down by not responding to any config cycles. In a system with two graphics chips, one on the motherboard, the other on add-in card, this strap can be used to disable one of the two through a jumper.	0 (the chip will respond)
WSDEGRADE	DVALID	Degrade workstation bonded part back to consumer level DEVICE_ID. See WSEN bonding option and DEVICE_ID table. This strap is don't care on parts with WSEN = 0. 0 = use workstation DEVICE_ID when WSEN=1 1 = use regular DEVICE_ID when WSEN=1	0

Table 4-28 Pin Based Straps (Continued)

Strap	Pin	Functional Description	Default
BUSCFG(2:0)	VID(6:4)	Controls bus type, CLK PLL select, and IDSEL. If AGP8X_DETb = 0: (both GC and MB 8x capable) 000 – AGP 8x, 0.8V signalling, PLL clk, IDSEL=AD16 001 – AGP 8x, 0.8V signalling, PLL clk, IDSEL=AD17 010 – AGP 4x, 0.8V signalling, PLL clk, IDSEL=AD16 011 – AGP 4x, 0.8V signalling, PLL clk, IDSEL=AD17 If AGP8X_DETb = 1: (either GC or MB not 8x capable) 000 – AGP 4x, PLL clk, IDSEL=AD16 001 – AGP 4x, PLL clk, IDSEL=AD17 010 – AGP 1x/2x, PLL clk, IDSEL=AD16 011 – AGP 1x/2x, PLL clk, IDSEL=AD17 100 – PCI 66 MHz, PLL clk 101 – PCI 33 MHz, 3.3V, REF clk 110 – AGP 1x, REF clk, IDSEL=AD16 111 – AGP 1x, REF clk, IDSEL=AD17 Notes: 1. For AGP configurations VID(4) acts as the IDSEL strap. For PCI it acts as the PLL bypass (33 or 66 MHz) strap. 2. AGP8X_DETb is either connected directly to MB_AGP8X_DET# (on agp connector) or made open via a 0 ohm resistor. The resistor is removed if we wish to enforce 1.5V signaling. Also note that **if this 0 ohm resistor is removed, so must be the 0 ohm resistor connecting GC_AGP8X_DET# to ground**. Otherwise the motherboard will operate with the wrong voltage levels.	000 (AGP 8x if MB capable, 4x if not)
AGPFBSKEW(1:0)	VID(1:0)	AGP 1x clock feedback phase adjustment wrt refclk (cpuclk) 00 – refclk slightly earlier than feedback 01 – refclk 1 tap earlier than feedback 10 – refclk 1 tap later than feedback 11 – refclk 2 taps earlier than feedback clock	00
X0CLK_SKEW(1:0)	VID(3:2)	Clock phase adjustment between x0clk (used for feedback) and agpclk 00 - 0 tap delay 01 - 1 tap delay 10 - 2 taps delay 11 - 3 taps delay	00 (no skew)
ROMIDCFG(3:0)	ROMCSb, ROMSO ROMSI ROMSCK ROMCSb is ROMIDCFG(3) ROMSO is ROMIDCFG(2) ROMSI is ROMIDCFG(1) ROMSCK is ROMIDCFG(0)	If no ROM attached, controls DEVICE_ID(1:0). If ROM attached, identifies ROM type and ROM will contain DEVICE_ID(1:0). See also *Table 4-29, "ROM Based Straps," on page 4-17*. 000x – No ROM, CHG_ID = 00 001x – No ROM, CHG_ID = 01 010x – No ROM, CHG_ID = 10 011x – No ROM, CHG_ID = 11 1000 – Parallel ROM on VID pins, CHG_ID in ROM 1001 – Serial AT25F1024, CHG_ID in ROM 1010 – Serial AT45DB011, CHG_ID in ROM 1011 – Serial ST Micro M25P10 / M25P05, CHG_ID in ROM 1100 – Serial ST Micro M25P05 1101 – Serial SST45LF010, CHG_ID in ROM 1110 – Parallel ROM on DVO pins, CHG_ID in ROM 1111 – Serial NexFlash NX25F011B / NX25F015B, CHG_ID in ROM. Support for these devices have been discontinued by NexFlash.	1000 (parallel ROM on VID)
VIP_DEVICE	VHAD(0)	Indicates if any slave VIP host port devices drove HAD(0) line low during reset. 0 – Slave VIP host port devices present. 1 – No slave VIP host port devices reporting presence during reset.	1

Notes on Pin Based Straps:

In order to better guarantee the proper latching of the straps on the VID(7:0), DVALID and PSYNC signals, even if there is an external device connected that does properly tri-state these signals during system reset, or if there is excessive leakage current, the use of on board LS244 buffers is recommended.

This circuit should not be needed if VID(7:0) are connected only to ATI devices, and not to any non-ATI devices and/or off board connectors or headers.

Also, note that most video decoders and external connectors/headers will only attach to VID(7:0). This means one octal LS244 buffer should be enough to force all 8 straps on these lines. DVALID and PSYNC are used only in a small subset of boards for MPEG transport stream capture. Only on these boards would LS244 buffers be needed on these two pins.

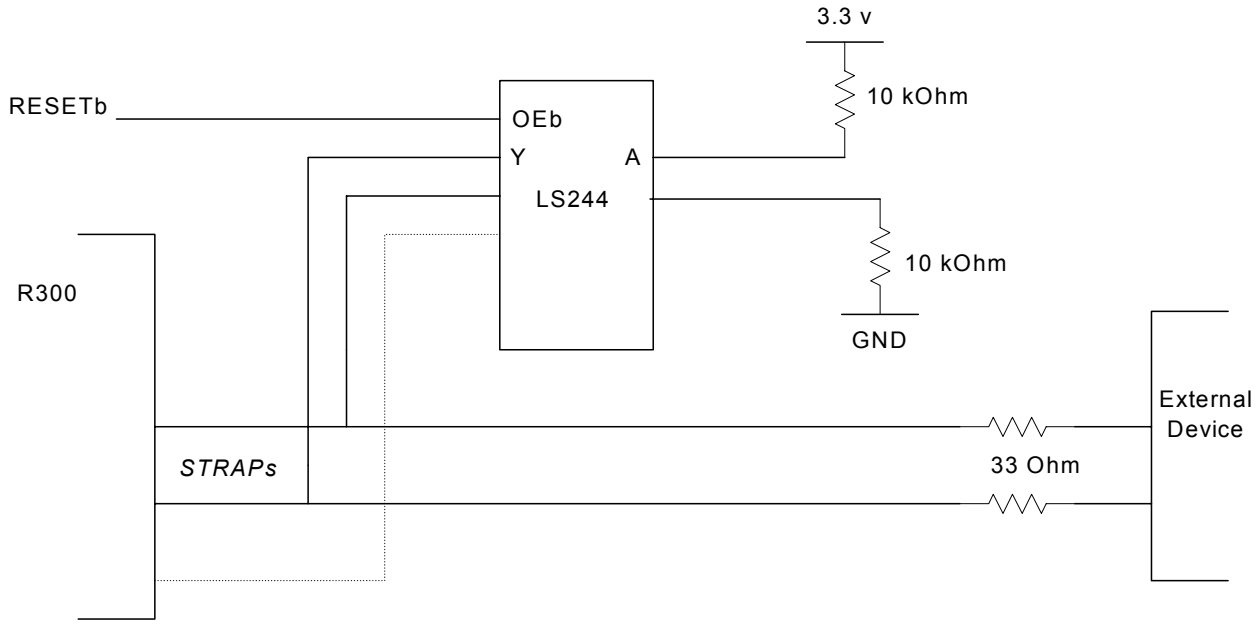

Figure 4-1 LS244 Strap Latching

If it is to be used off the circuit board, the STEREOSYNC pin should be buffered with an LS125, or equivalent. e.g. if the VESA Stereo display connector is populated. This will prevent external devices from interfering with the strap value floating according to the internal pull-down and potential external pull-up during reset. If STEROSYNC is not used in a given board design, then the LS125 is not required.

For straps which must be set on the board, the use of 4.7 kohm (Min) to 10 kohm (Max) resistors is recommended (for pull-ups to power (3.3V) or pull downs to ground). 4.7 kohm provides more noise immunity whereas 10 kohm will result in lower static power dissipation.

Board level strap resistors should always be installed. The internal logic may not implement a default pull-up or pull-down, as it assumes an external strap is always populated. This prevents current paths to ground in the case where the desired strap value is not the typical default value.

4.2.2 ROM Based Straps

If a ROM is attached (see ROMIDCFG pin based straps), then after RSTb goes inactive (high) the ROM is read at the addresses listed below to default these internal settings.

If there is a ROM attached, but the byte at address 0x1 of the ROM is not equal to 0xAA, then the ROM is considered blank (un-programmed) and the ASIC defaults to the “no ROM” case. This situation will only occur during add-in board production, prior to the BIOS ROM being flashed for the first time.

Table 4-29 ROM Based Straps

Strap	ROM Location	Functional Description	ASIC Default If No ROM
BLANK_ROM	Byte 0x01, Bits 7:0	If this byte = 0xAA, then ROM is not blank and all other ROM based straps are read. If this byte is not 0xAA, the ROM is considered blank and no more ROM based straps are read. No ROM defaults are used.	Blank ROM
AGPVCOGAIN(2:0)	Byte 0x70, Bits 2:0	AGP PLL VCO gain control. iPVG(2:0) on macro. If no ROM, then default taken from bonding options and register defaults.	Bit 2:1 from bonding opt, Bit 0 from register default
AGPCPGAIN(2:0)	Byte 0x70, Bits 6:4	AGP PLL charge pump gain control. iPCP(2:0) on the macro. If no ROM, then default taken from bonding options and register defaults.	Bit 2:1 from bonding opt, Bit 0 from register default
apad_strength3_3V	Byte 0x71	Controls default impedance of AGP/PCI pads for PCI, AGP 1x and AGP 2x (3.3V environments) Bits 7:4 N-MOS impedance control Bits 3:0 P-MOS impedance control	PCI: 0x52 AGP 1x: 0x52 AGP 2x: 0x52
apad_strength1_5V	Byte 0x72	Controls default impedance of AGP/PCI pads for AGP 4x (1.5V environment) Bits 7:4 N-MOS impedance control Bits 3:0 P-MOS impedance control	AGP 4x: 0x28
apad_strength0_8V	Byte 0x73	Controls default impedance of AGP/PCI pads for AGP 8x (0.8V signalling) Bits 7:4 N-MOS impedance control Bits 3:0 P-MOS impedance control	AGP 8x: 0x37
CHG_ID(1:0)	Byte 0x74, Bit 1:0	Selects PCI DEVICE_ID(1:0). 00 = DEVICE_ID(1:0) = 00 01 = DEVICE_ID(1:0) = 01 10 = DEVICE_ID(1:0) = 10 11 = DEVICE_ID(1:0) = 11 If no ROM attached, see ROMIDCFG pin based straps. See AGP function table below for detail on effect on AGP ability claim.	From ROMIDCFG pin based straps
FAST_WT_DISABLE	Byte 0x74 Bit 2	Disable AGP fast write	0
EXT_MEM_EN	Byte 0x74 Bit 3	Extended memory (4G) enable	0
AP_SIZE(1:0)	Byte 0x74, Bits 5:4	Size of the primary memory apertures claimed in PCI configuration space. 00 = 2 x 64 MB 01 = 2 x 128 MB 10 = 2 x 32 MB 11 = 2 x 256MB If no ROM the default is 00 = 2 x 64 MB.	00
MULTI_FUNC(1:0)	Byte 0x74, Bits 7:6	Multi-function device select 00 = single function device. 01 = two function device. No AGP in either function 10 = two function device. AGP only in function 0 11 = two function device. AGP in both functions If BUSCFG pin based straps are set to PCI, then AGP will not be enabled in any function. See AGP function table below for detail on AGP ability claims. See DEVICE_ID table in section A.2 for more detail on DEVICE_ID values for the second PCI function.	00
ENINTb	Byte 0x75 Bit 0	0- Enables interrupt 1- Disables interrupt	0 (enable)
vga_disable	Byte 0x75 Bit 1	0- VGA controller capability enabled. 1- The device will not be recognized as the system's VGA controller.	0 (enable)
EMU_DESKTOP	Byte 0x75 Bit2	0: No affect on mobile enable. 1: Forces mobile enabled parts to emulate desktop. Always set low in desktop BIOS. Always set high in mobile BIOS. Allows desktop BIOS loaded on mobile enabled parts to put chip into desktop mode.	0 (enable)
HDCP_DISABLE	Byte 0x75 Bit 3	Disable HDCP	0

Table 4-29 ROM Based Straps (Continued)

Strap	ROM Location	Functional Description	ASIC Default If No ROM
MV_DISABLE	Byte 0x75 Bit 4	Disable Macrovision	0
SLAVE_DAC_DECODE	Byte 0x75 Bit 5	Decode Dual Address Slave Cycle and using 64bit bar	0
MSI_ENABLE	Bit 6	Enable Message Signalled Interrupt	0
BM_DAC_EN	Bit 7	Enable Dual Address Bus Mastering Cycle	0
SUBSYS_VEN_ID(15:0)	Byte 0x76- 0x77	Sub-System Vendor ID (SSVID) for PCI configuration space. If no ROM attached, then for motherboard system ROM writes in the SSVID **before** the enumeration cycle is initiated, else for dual-chip card, slave chip uses 0x1002 as SSVID.	1002h (i.e. ATI)
SUBSYS_ID(15:0)	Byte 0x78- 0x79	Sub-System ID (SSID) for PCI configuration space. If no ROM attached, then for motherboard system ROM writes in the SSID **before** the enumeration cycle is initiated, else for dual-chip card, slave chip uses DEVICE_ID as SSID.	Same as DEVICE_ID. See CHG_ID.

Table 4-30 below details how the AGP ability is claimed in each PCI function space:

Table 4-30 AGP Function Claim In PCI Configuration Space

BUSCFG(2:0)	MULTI_FUNC(1:0)	CHG_ID(1:0)	Function 0 AGP	Function 1 AGP
PCI 66 or PCI 33	X	X	No AGP	No AGP
Any AGP	11	X	Claim AGP	Claim AGP
Any AGP	10	X	Claim AGP	No AGP
Any AGP	01	X	No AGP	No AGP
Any AGP	00	00, 01 or 10	Claim AGP	No AGP
Any AGP	00	11	No AGP	No AGP

All pin, ROM and bonding straps can be read back from internal registers so that software may examine them. *Table 4-31* below lists the location of all these register fields. The exception is ID_DISABLE, which has no readback since it is zero by definition if the chip responds to PCI/AGP requests.

Table 4-31 Register Fields

Strap	Read	Write	Default
VGA_DISABLE	CONFIG_XSTRAP(0)	No write	ROM: from ROM No ROM: “0”
MOBILE_EN	CONFIG_XSTRAP(1)	No write	From bonding pin
BLANK_ROM	CONFIG_XSTRAP(2)	No write	ROM: 0 if byte 1=0xAA, else 1 No ROM: “1”
ENINTb	CONFIG_XSTRAP(3)	No write	ROM: from ROM No ROM: “0”
MULTI_FUNC(1:0)	CONFIG_XSTRAP(5:4)	No write	ROM : from ROM No ROM: “00”
AGPSKEW(1:0)	CONFIG_XSTRAP(7:6)	No write	From pins
X0CLK_SKEW(1:0)	CONFIG_XSTRAP(9:8)	No write	From pins
ID_DISABLE	CONFIG_XSTRAP(10)	No write	ROM : from ROM No ROM: “0”
VIP_DEVICE	CONFIG_XSTRAP(13)	No write	From pin
EMU_DESKTOP	CONFIG_XSTRAP(14)	No write	ROM : from ROM No ROM: “0”
EXT_MEM_EN	CONFIG_XSTRAP(15)	No write	ROM: from ROM No ROM: “0”
AP_SIZE(1:0)	CONFIG_XSTRAP(17:16)	No write	ROM: from ROM No ROM: “00”

Table 4-31 Register Fields (Continued)

Strap	Read	Write	Default
CHG_ID(1:0)	CONFIG_XSTRAP(19:18)	No write	ROM: from ROM No ROM: from ROMSO & ROMSI pin straps
ROMIDCFG(3:0)	CONFIG_XSTRAP(23:20)	No write	From pins
BUSCFG(2:0)	CONFIG_XSTRAP(26:24)	No write	From pins
WSEN	CONFIG_XSTRAP(27)	No write	From bonding pin
WSDEGRADE	CONFIG_XSTRAP(28)	No write	From pin
HDCP_DISABLE	CONFIG_XSTRAP(29)	No write	ROM: from ROM No ROM: “0”
FAST_WT_DISABLE	CONFIG_XSTRAP(30)	No write	ROM: from ROM No ROM: “0”
MV_DISABLE	CONFIG_XSTRAP(31)	No write	ROM: from ROM No ROM: “0”
BM_DAC_EN	CONFIG_XSTRAP2(0)	No write	ROM : from ROM No ROM: “0”
AGP8X_DETb	CONFIG_XSTRAP2(1)	No write	ROM : from ROM No ROM: “0”
SLAVE_DAC_DECODE	CONFIG_XSTRAP2(2)	No write	ROM : from ROM No ROM: “0”
MSI_ENABLE	CONFIG_XSTRAP2(2)	No write	ROM : from ROM No ROM: “0”
SUBSYS_VEN_ID(15:0)	PCICFG 0x2C-0x2D	PCICFG 0x4C-0x4D	ROM: from ROM No ROM: 0x1002
SUBSYS_ID(15:0)	PCICFG 0x2E-0x2F	PCICFG 0x4E-0x4F	ROM: from ROM No ROM: DEVICE_ID
APD_STRENGTH	PAD_CTLR_STRENGTH	Use PAD_MANUAL_OVERRIDE function	ROM: from ROM No ROM PCI: 0xF5 No ROM AGP 1x/2x: 0x77 No ROM AGP 4x: 0x8E
AGPVCOGAIN(2:1)	APLL_VCO_GAIN(2:1)	Can write	From bonding pins
AGPVCOGAIN(0)	APLL_VCO_GAIN(0)	Can write	1
AGPCPGAIN(2:1)	APLL_PUMP_GAIN(2:1)	Can write	From bonding pins
AGPCPGAIN(0)	APLL_PUMP_GAIN(0)	Can write	0

4.2.3 Board Level ROM Wiring

The RADEON 9800 supports parallel ROM on either the TVODATA pins, or the DVODATA pins, as selected by the ROMIDCFG straps (see pin based straps).

If either the TVO port or the DVO port are used on a board for another purpose besides parallel ROM (e.g. video encoder, or SDR DVO, or dual channel DVO), then those pins should not be used for parallel ROM. If both sets of pins are used on a board design, then a serial ROM must be used. See *Table 4-32* below for details:

Table 4-32 Serial ROM

Signal Name	Serial ROM
ROMCSb	CSb
ROMSI	SI
ROMSO	SO
ROMSCK	SCK

To use parallel ROM on TVO pins a board must have VDDR2 = 3.3V and TVOVMODE = 0V.

Due to pin constraints, the two external octal flops are needed to latch the lower 16 bits of the ROM address. *Figure 4-2* below shows the connection for a 128k parallel ROM. 64k ROM connection is the same except that the A(16) to ROMSI

connection is not needed.

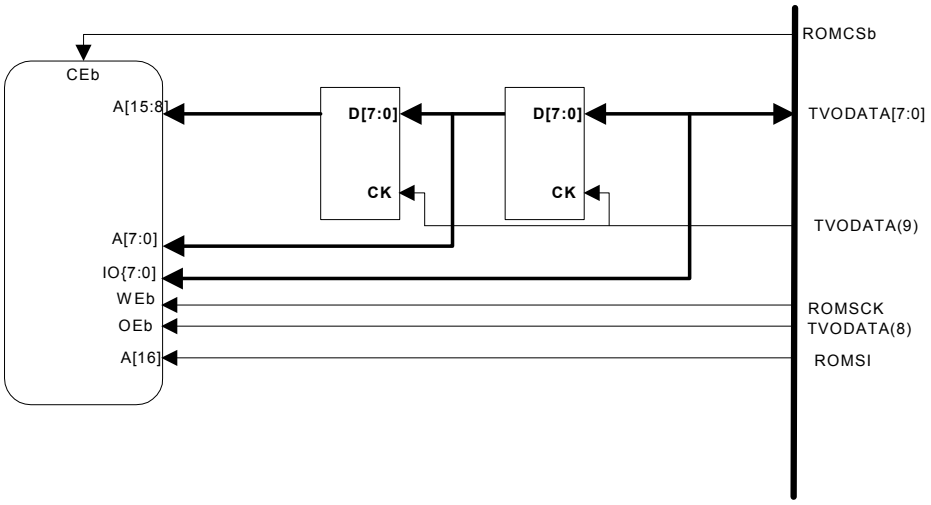

Figure 4-2 128K Configuration

Table 4-33 below summarizes the parallel ROM connection on the TVO pins for EPROM and FLASHROM of 64k and 128k.

Table 4-33 Parallel ROM Connection On TVO Pins

Signal Name	PROM/EPROM		Flash ROM	
	64kB	128kB	64kB	128kB
Muxed on TVODATA(7:0)	A(7:0)	A(7:0)	A(7:0)	A(7:0)
	A(15:8)	A(15:8)	A(15:8)	A(15:8)
ROMSI	N/A	A(16)	N/A	A(16)
Muxed on TVODATA(7:0)	D(7:0)	D(7:0)	D(7:0)	D(7:0)
TVODATA(8)	OEb	OEb	OEb	OEb
ROMCSb	CEb	CEb	CEb	CEb
ROMSCK	N/A	N/A	WEb	WEb
TVODATA(9)	CLK	CLK	CLK	CLK

Table 4-34 below summarizes the parallel ROM connection on the DVO pins for EPROM and FLASHROM of 64k and 128k.

Table 4-34 Parallel ROM Connection On DVO Pins

Signal Name	PROM/EPROM		Flash ROM	
	64kB	128kB	64kB	128kB
Muxed on DVODATA(0:7)	A(7:0)	A(7:0)	A(7:0)	A(7:0)
	A(15:8)	A(15:8)	A(15:8)	A(15:8)
ROMSI	N/A	A(16)	N/A	A(16)
Muxed on DVODATA(0:7)	D(7:0)	D(7:0)	D(7:0)	D(7:0)
DVODATA(8)	OEb	OEb	OEb	OEb
ROMCSb	CEb	CEb	CEb	CEb
ROMSCK	N/A	N/A	WEb	WEb
DVODATA(9)	CLK	CLK	CLK	CLK

The RADEON 9800 and R200 have opposite mapping of the ROM pins to the DVODATA(7:0) pins. On RADEON 9800 ROM pins A(7:0), A(15:8) and D(7:0) map to DVODATA(0:7) in reverse numerical order. Therefore:

- A(0), A(8) and D(0) are on DVODATA(7)
- A(7), A(15) and D(7) are on DVODATA(0)

This is done to simplify board level routing of these 8 wires, which had to all cross each other with the R200 pinout ordering.

Refer to *Figure 4-3* and *Figure 4-4* below for Read and Write operations for 128k EPROM/FLASHROM:

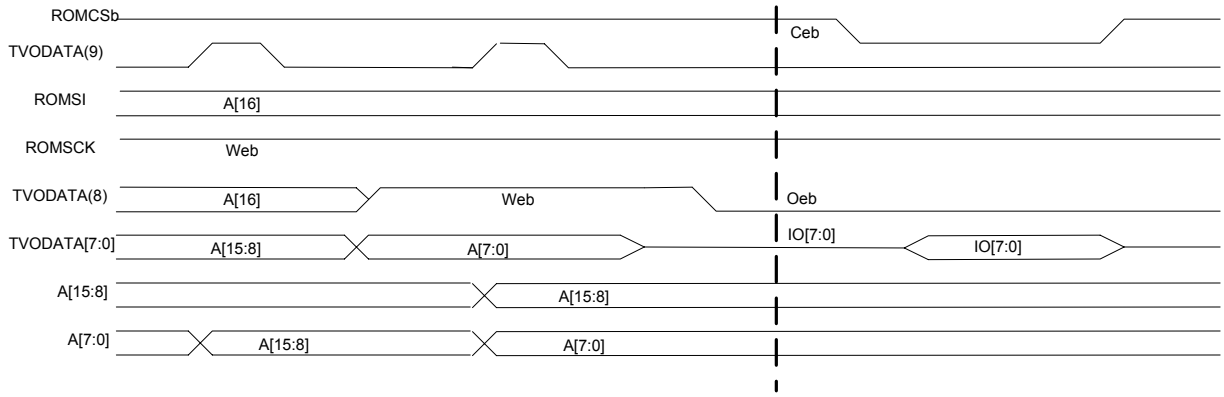

Figure 4-3 ROM Read

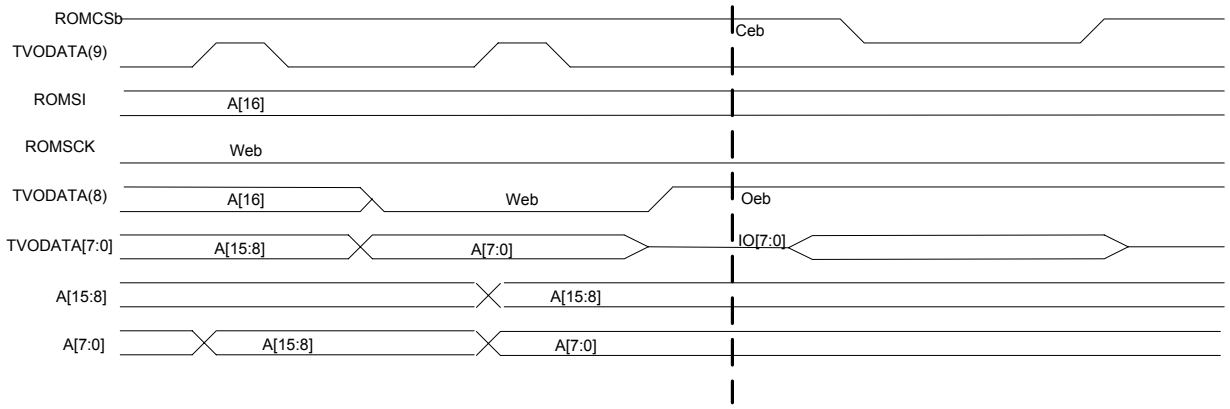

Figure 4-4 ROM Write

4.3 RADEON 9800 Pin Assignment Top-View

Table 4-35 Legend for RADEON 9800 Pin Assignment Top View

Category	Color
memory	
VSS	
VDDC	
VDDR1	
VDDC18	
VDDR2/3/4	
DVO, TVO	
DAC1	
DAC2	
miscellaneous	
TMDS	
ROM	
VDDP	
VIP Video Capture	
VSSP	
AGP	
VDDCI	

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
A		DQC28	QSC3	DQC27	DQC25	DQB55	DQB53	QSB6	DQB51	DQB49	DQB39	DQB37	QSB4	DQB35	DQB33	CASB#	CKEB	MAB12	CLKB1#
B	DQC29	VSS	DQMC#3	DQC26	DQC24	DQB54	DQB52	DQMB#6	DQB50	DQB48	DQB38	DQB36	DQMB#4	DQB34	DQB32	WEB#	CSB#	MAB7	CLKB1
C	DQC31	DQC30	VSS	DQC17	DQC16	MPVSS	MPVDD	DQB63	VSS	DQMB#7	DQB58	DQB47	VSS	DQMB#5	DQB42	VSS	MAB13	MAB0	MAB1
D	DQC9	DQC8	DQC19	VSS	DQC18	VDDR1	VSS	DQB62	DQB60	DQB59	DQB57	DQB46	DQB44	DQB43	DQB41	RASB#	MAB8	MAB6	MAB5
E	DQC11	DQC10	QSC2	DQMC#2	VSS	DQC20	MEMVMODE0	DQB61	QSB7	VSS	DQB56	DQB45	QSB5	VSS	DQB40	DIMB1	MAB14	VSS	MAB2
F	QSC1	DQMC#1	VSS	DQC22	DQC21	VSS	MEMVMODE1	VSS	TEST_MCLK	VSS	VDDR1	VDDR1	VSS	VDDR1	VSS	VDDR1	VDDR1	VSS	VDDR1
G	DQC13	DQC12	DQC1	DQC0	DQC23	TEST_YCLK	VSS	VDDR1	VSS	VDDR1	VDDR1	VSS	VDDR1	VDDR1	VSS	VSS	VDDR1	VDDR1	VSS
H	DQC15	DQC14	DQMC#0	DQC3	DQC2	VSS	VDDR1												
J	DIMC0	CLKC0#	DQC5	DQC4	QSC0	VSS	VDDR1												
K	CLKC0	VSS	DQC7	DQC6	VSS	VDDR1	VSS												
L	CLKC1#	CLKC1	MAC9	MAC10	MAC11	VDDR1	VDDRH												
M	MAC5	MAC2	MAC4	MAC3	VDDR1	VSS	VSSRH												
N	MAC7	MAC0	VSS	MAC6	MAC1	VSS	VDDC18						VDDC	VDDC	VDDC	VDDC	VDDC	VSS	VSS
P	DQC33	DQC32	MAC13	MAC8	MAC12	MAC14	VSS						VDDC	VDDC	VDDC	VDDC	VDDC	VSS	VSS
R	DQC35	DQC34	CSC#	RASC#	CKEC	VDDR1	VSS						VDDC	VDDC	VDDC	VDDC	VDDC	VSS	VSS
T	QSC4	DQMC#4	VSS	CASC#	WEC#	VSS	VDDR1						VDDC	VDDC	VDDC	VDDC	VDDC	VSS	VSS
U	DQC37	DQC36	DQC41	DQC40	DIMC1	VSS	VDDR1						VDDC	VDDC	VDDC	VDDC	VDDC	VSS	VSS
V	DQC39	DQC38	DQMC#5	DQC43	DQC42	VDDR1	VDDR1						VSS	VSS	VSS	VSS	VSS	VSS	VSS
W	DQC49	DQC48	DQC44	QSC5	VSS	VDDR1	VSS						VSS	VSS	VSS	VSS	VSS	VSS	VSS
Y	DQC51	DQC50	VSS	DQC46	DQC45	VSS	VSS						VSS	VSS	VSS	VSS	VSS	VSS	VSS
AA	QSC6	DQMC#6	DQC57	DQC56	DQC47	VDDR1	VDDR1						VSS	VSS	VSS	VSS	VSS	VSS	VSS
AB	DQC53	DQC52	DQMC#7	DQC59	DQC58	VDDR1	VDDR1						VSS	VSS	VSS	VSS	VSS	VSS	VSS
AC	DQC55	DQC54	DQC60	QSC7	VSS	VREF1	VSS						VDDC	VDDC	VDDC	VDDC	VDDC	VSS	VSS
AD	DQD25	DQD24	VSS	DQC62	DQC61	VDDR1	VSS						VDDC	VDDC	VDDC	VDDC	VDDC	VSS	VSS
AE	DQD27	DQD26	DQD17	DQD16	DQC63	VDDR1	VSS						VDDC	VDDC	VDDC	VDDC	VDDC	VSS	VSS
AF	QSD3	DQMD#3	DQMD#2	DQD19	DQD18	VSS	VDDR1						VDDC	VDDC	VDDC	VDDC	VDDC	VSS	VSS
AG	DQD29	DQD28	DQD20	QSD2	VT1	VSS	VDDR1						VDDC	VDDC	VDDC	VDDC	VDDC	VSS	VSS
AH	DQD31	DQD30	VSS	DQD22	DQD21	VT2	VSS												
AJ	DQD9	DQD8	DQD1	DQD0	DQD23	VDDR1	VSS												
AK	DQD11	DQD10	DQMD#0	DQD3	DQD2	VSS	VDDC18												
AL	QSD1	DQMD#1	DQD4	QSD0	VSS	VDDR1	VDDRH												
AM	DQD13	DQD12	VSS	DQD6	DQD5	VDDR1	VSSRH												
AN	DQD15	DQD14	MAD10	MAD11	DQD7	VDDR1	VDDC	VDDR1	VDDR1	VSS	VSS	VDDR1	VDDR1	VDDR1	VSS	VSS	VDDR4	VDDR4	VSS
AP	DIMD0	CLKD0#	MAD3	MAD9	VSS	VDDC	VDDR1	VDDR1	VSS	VDDR1	VDDR1	VDDR1	VSS	VSS	VDDR4	VDDR4	VSS	VSS	VDDR2
AR	CLKD0	VSS	MAD5	MAD2	VDDC	MAD4	DIMD1	DQD42	QSD5	DQD45	DQD56	VSS	QSD7	DQD61	DVODATA1	VDDR4	DVODATA8	VSS	TVOVMODE
AT	CLKD1#	CLKD1	MAD0	VDDC	MAD6	MAD1	DQD40	DQD43	DQD44	DQD46	DQD57	DQD59	DQD60	DQD62	DVODATA0	DVODATA5	DVODATA7	DVOVMODE	TVODATA3
AU	MAD13	MAD8	VDDC	MAD12	MAD7	VSS	DQD41	DQMD#5	VSS	DQD47	DQD58	DQMD#7	VSS	DQD63	DVOCNTL0	DVODATA4	DVODATA6	DVODATA11	TVODATA2
AV	CKED	VDDC	CSD#	MAD14	DQD32	DQD34	DQMD#4	DQD36	DQD38	DQD48	DQD50	DQMD#6	DQD52	DQD54	DVOCNTL1	DVODATA3	DVOCLK1	DVODATA10	TVODATA1
AW		CASD#	WED#	RASD#	DQD33	DQD35	QSD4	DQD37	DQD39	DQD49	DQD51	QSD6	DQD53	DQD55	DVOCNTL2	DVODATA2	DVOCLK0	DVODATA9	TVODATA0
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19

Figure 4-5 RADEON 9800 Pin Assignment Top-View (Left Side)

20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	
CLKB0	DIMB0	DQB15	DQB13	QSB1	DQB11	DQB9	DQB31	DQB29	QSB3	DQB27	DQB25	DQA55	DQA53	QSA6	DQA51	DQA49	DQA39	DQA37		A
VSS	CLKB0#	DQB14	DQB12	DQMB#1	DQB10	DQB8	DQB30	DQB28	DQMB#3	DQB26	DQB24	DQA54	DQA52	DQMA#6	DQA50	DQA48	DQA38	DQA36	QSA4	B
MAB4	MAB9	DQB7	VSS	DQMB#0	DQB2	DQB23	VSS	DQMB#2	DQB18	DQA63	VSS	DQMA#7	DQA58	DQA47	VSS	DQMA#5	VSS	DQMA#4	DQA35	C
MAB3	MAB10	DQB6	DQB4	DQB3	DQB1	DQB22	DQB20	DQB19	DQB17	DQA62	DQA60	DQA59	DQA57	DQA46	DQA44	DQA43	DQA41	DQA34	DQA33	D
VSS	MAB11	DQB5	QSB0	VSS	DQB0	DQB21	QSB2	VSS	DQB16	DQA61	QSA7	VSS	DQA56	DQA45	QSA5	DQA42	DQA40	DQA32	CASA#	E
VDDR1	VDDR1	VDDR1	VSS	MEMTEST	VDDR1	VSS	VDDR1	VDDR1	VSS	VSS	VDDR1	VDDR1	VDDR1	DIMA1	VSS	WEA#	CSA#	CKEA	RASA#	F
VDDC184	VSSRH	VDDRH	VDDR1	VREF2	VDDR1	VDDR1	VSS	VSS	VDDR1	VDDR1	VSS	VDDR1	VDDR1	MAA14	MAA12	MAA8	MAA13	CLKA1	CLKA1#	G
													VDDR1	VDDR1	MAA6	MAA0	MAA7	VSS	CLKA0	H
													VDDC18	VSS	MAA2	MAA5	MAA1	CLKA0#	DIMA0	J
													VSS	VSS	VSS	MAA3	MAA4	DQA14	DQA15	K
													VDDRH	VDDR1	MAA11	MAA10	MAA9	DQA12	DQA13	L
													VSSRH	VDDR1	DQA5	DQA6	DQA7	DQMA#1	QSA1	M
VSS	VSS	VSS	VDDCI	VDDC	VDDC	VDDC	VDDC						VSS	VDDR1	QSA0	DQA4	VSS	DQA10	DQA11	N
VSS	VSS	VSS	VDDC	VDDC	VDDC	VDDC	VDDC						VSS	VSS	VSS	DQA3	DQMA#0	DQA8	DQA9	P
VSS	VSS	VSS	VDDC	VDDC	VDDC	VDDC	VDDC						VDDR1	VSS	DQA0	DQA1	DQA2	DQA30	DQA31	R
VSS	VSS	VSS	VDDC	VDDC	VDDC	VDDC	VDDC						VDDR1	VDDR1	DQA21	DQA22	DQA23	DQA28	DQA29	T
VSS	VSS	VSS	VDDC	VDDC	VDDC	VDDC	VDDC						VSS	VDDR1	QSA2	DQA20	VSS	DQMA#3	QSA3	U
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						VDDR1	VSS	VSS	DQA19	DQMA#2	DQA26	DQA27	V
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						VDDR1	VDDR1	DQA16	DQA17	DQA18	DQA24	DQA25	W
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						VDDP	VSSP	VSSP	AD0	AD1	VSSP	AD16	Y
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						VDDP	VSSP	PAR	AD2	AD3	AD18	CBE#2	AA
VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS						VDDP	VDDP	STOP#	AD4	AD5	AD20	AD17	AB
VSS	VSS	VSS	VDDC	VDDC	VDDC	VDDC	VDDCI						VDDP	VSSP	VSSP	AD6	VSSP	AD22	AD19	AC
VSS	VSS	VSS	VDDC	VDDC	VDDC	VDDC	VDDC						VDDP	VSSP	DEVSEL#	AD_STBS0	AD7	CBE#3	AD21	AD
VSS	VSS	VSS	VDDC	VDDC	VDDC	VDDC	VDDC						VDDP	VSSP	TRDY#	VSSP	AD_STBF0	AD_STBS1	AD23	AE
VSS	VSS	VSS	VDDC	VDDC	VDDC	VDDC	VDDC						VDDP	VDDP	VSSP	CBE#0	AD8	VSSP	AD_STBF1	AF
VSS	VSS	VSS	VDDCI	VDDC	VDDC	VDDC	VDDC						VDDP	AGPREF	FRAME#	AD9	AD10	AD25	AD24	AG
													VDDP	VSSP19	IRDY#	AD11	AD12	AD27	AD26	AH
													VDDP	VDDP	VSSP	AD13	VSSP	AD29	AD28	AJ
													VDDP	VSSP	VSSP	AD15	AD14	AD31	AD30	AK
													VDDP	VSSP	AGP8X_DET#	AGPTEST	CBE#1	DBI_HI	DBI_LO	AL
													VSSP	VDDP	VSSP	WBF#	VSSP	VSSP	RBF#	AM
VSS	VDDR2	VDDC18	VSS	VSS	VDDR3	VSS	VDDC18	VDDR3	VDDR3	VSS	VSS	VDDC18	VDDP	VDDP	VSSP	SBA6	SBA7	ST2	ST1	AN
VDDR2	VSS	VSS	VSS	VDDR3	VSS	VDDR3	VDDR3	VSS	ROMSO	ROMSCK	AUXWIN	STEREOSYNC	TEST_AGPCLK	VSS184	RST#	SBA4	SBA5	GNT#	ST0	AP
VSS	VSS	VDDR3	VDDR3	AVSSN1	VDDR3	VSS	SCL	SDA	ROMSI	ROMCS#	HPD1	H2SYNC	HPD2	DDC2CLK	DDC2DATA	VSSP	SB_STBS	SB_STBF	SBA3	AR
TVODATA7	TVODATA9	VSS	VSS	AVSSN2	A2VSSN1	VSS2DI	A2VSSQ	TXVDDR2	TXVDDR1	VSYNC	HSYNC	V2SYNC	VHAD1	VID7	VID3	TESTEN	SBA0	SBA1	SBA2	AT
TVODATA6	TVODATA8	AVSSQ	VDD1DI	VSS1DI	A2VDDQ	A2VSSN2	VDD2DI	TXVSSR1	TXVSSR2	TXVSSR3	DDC1CLK	DDC1DATA	VHAD0	VID6	VID2	DVALID	INTA#	VSSP1	REQ#	AU
TVODATA5	TVOCLKI	RSET	AVDD1	AVDD2	R2SET	A2VDD1	A2VDD2	TPVSS	TXCM	TX0M	TX1M	TX2M	VIPCLK	VID5	VID1	PSYNC	PVSS	XTALIN	PCICLK	AV
TVODATA4	TVOCLKO	B	G	R	COMP_B	Y_G	C_R	TPVDD	TXCP	TX0P	TX1P	TX2P	VPHCTL	VID4	VID0	VPCLK0	PVDD	XTALOUT		AW
20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	

Figure 4-6 RADEON 9800 Pin Assignment Top-View (Right Side)

Chapter 5
Electrical Characteristics

All voltages are with respect to VSS unless specified otherwise.

5.1 Maximum Rating Conditions

Note: These are stress ratings only, i.e., operation of the device at these conditions is not implied. Ratings are referenced to VDD. Any stress greater than the *absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect the device reliability.

Table 5-1 Maximum Rated Conditions

Item	Value
I/O Supply Voltage	-0.35V to +3.60V *
Core or Analog Supply Voltage	0 to 2.0V
A2VDD	0 to 2.75V
VDDP (3.3V)	0 to 3.9V
Input or Output Voltage	-0.35 to 1.8V
DC Forward Bias Current	-12mA (source), +24mA (sink)
Note *: core VDD stable	

5.2 Recommended DC Operating Conditions

Table 5-2 Recommended DC Operating Conditions

Item	Value
Memory I/O Supply (VDDR1)	2.5V / 1.8V ± 5%
DVO/TVO/Parallel ROM I/O Supply (VDDR2)	3.3 V/ 1.8 V ± 5%
GPIO I/O Supply (VDDR3)	3.3 V ± 5%
DVO/Parallel ROM I/O Supply (VDDR4)	3.3 V/1.8 V ± 5%
Special I/O Supply (VDDC18)	1.8 V ± 5%
TMDS PLL Supply (TPVDD)	1.8 V ± 5%
TMDS Macro Supply (TXVDDR)	1.8 V ± 5%
Memory PLL Supply (MPVDD)	1.8 V ± 5%
Memory CLK I/O Supply (VDDRH1,VDDRH2)	2.5V / 1.8V ± 5%
PCI/AGP I/O Supply (VDDQ)	AGP/PCI ± 5% (3.3 V / 1.5 V)
Digital Core Supply (VDDC)	1.5 V to 1.77V ± 5%
PLL Supply (PVDD)	1.8 V ± 5%
DAC Digital Supply (VDDD1)	1.8 V ± 5%
Analog (DAC) Supply (AVDD)	1.8 V ± 5%
A2VDD Dedicated Power for TV DAC	2.5V ± 5%
A2VDDQ Dedicated Power for TV DAC	1.8 V ± 5%

5.3 Power Consumption

The table below shows the measured maximum current consumption for each power group, using an ATI test board, under the following conditions: 256MB configuration (using Hynix 400MHz 8x32 DDR-1 memories), and engine/memory speeds set at 412/365MHz. These measured values are given as guidelines for sizing regulators only; it is understood that they may vary depending on the design and the engine/ memory speed of the actual board.

Table 5-3 Power Consumption by Power Group

Power Group	Voltage (V)	Maximum Current (mA)
VDDR1	2.65	1.28
AVDD	1.8	0.10
VDDC_CT (Core Transform)	1.9	0.45
TPVDD	1.8	0.03
TXVDDR	1.8	0.03
PVDD	1.8	0.03
AVDDI	1.8	0.03
A2VDD	2.5	0.15
A2VDDI	1.8	0.03
A2VDDQ	1.8	0.02
MPVDD	1.8	0.02
VDDR3 (I/O)	3.3	0.01
VDDR2 (DVO)	3.3	0.01
VDDR4 (TVO)	3.3	0.01
VDDC	1.77	24.50
Vtt	1.4	0.00
Fan	12	0.23

5.4 TTL Interface

Table 5-4 TTL Interface (GPIOs)

Parameter	Condition	Min.	Typical	Max.
VIL - Low Level Input Voltage	-	-	-	0.8 V
VIH - High Level Input Voltage	-	2.0 V	-	-
VOL - Low Level Output Voltage	IOL = 14 mA	-	0.2 V	0.4 V
VOH - High Level Output Voltage	IOH = 23 mA	2.4 V	3.4 V	-

5.5 General Electrical Characteristics

Table 5-5 below applies to all signals in the chip.

Table 5-5 General Electrical Characteristics

Parameter	Condition	Min.	Typical	Max.
IIL - Low Level Input Current	VI = VSS	-	-	-1 μA *
IIH - High Level Input Current	VI = VCC	-	-	+1 μA
IOZ - Tristate Output Leakage	VO = 0 V or VCC	-	-	± 1μA
CIN - Input Capacitance	Freq = 1 MHz @ 0 V	-	4 pF	8 pF
CO - Output Capacitance	Freq = 1 MHz @ 0 V	-	6 pF	-
CIO - Bidirectional I/O Capacitance	Freq = 1 MHz @ 0 V	-	6 pF	10 pF
IKLU - I/O Latch-up Current	V<VSS, V>VCC	100 mA	-	-
VEPO - Electrostatic Protection	C=100 pF R=1.5 kΩ	2 kV	-	-

* Current into chip is defined positive

5.6 Memory Interface Electrical Characteristics

Table 5-6 Memory Interface LVTTL Interface

Parameter	Condition	Min.	Max.
VIL - Low Level Input Voltage	Vout ≥ VOH(min) or Vout ≤ VOL(max)	-0.3 V	0.8 V
VIH - High Level Input Voltage		2.0 V	VDD-0.3 V
IIN - Input current	Vin=0 or Vin=VDD *		±10 μA
VOL - Low Level Output Voltage	VDD= min, IOL = 2mA		0.4 V
VOH - High Level Output Voltage	VDD = min, IOH = -2mA	2.4 V	

* Excluding common Input/Output terminals

Table 5-7 Memory Interface For Matched Impedance (60 Ohm/1.8V)

Parameters	Min	Norm	Max
VDDQ - I/O Power supply voltage	1.7V	1.8V	1.9V
VREF - Reference voltage	0.49 x VDDQ	0.90V	0.51 x VDDQ
VIH - Input logic high voltage, DC	VREF + 0.15V		VDDQ + 0.3V
VIL - Input logic low voltage, DC	VSSQ - 0.3V		VREF - 0.15V
VOH - Output logic high voltage (IoH = -7.47mA)	VDDQ - 0.5V		
VOL - Output logic low voltage (IoL = 7.47mA)			0.5V
VIH - Input logic high voltage, AC DDR	VREF + 0.3V		VDDQ + 0.3V
VIL - Input logic low voltage, AC DDR	VREF - 0.3V		VSSQ - 0.3V
VID - Clock differential input voltage (CLK/CLK#)	0.6V		VDDQ + 0.6V
VIX - Clock input crossing point (CLK/CLK#)	VREF - 0.15V	VREF	VREF + 0.15V

Table 5-8 Memory Interface Electrical Characteristics SSTL

Symbol	Parameter	SSTL-2		
		Min	Norm	Max
VDDC (Core Supply)	Device voltage supply		1.5V	1.8V
VDDR (I/O Supply)	Output voltage supply	2.3V	2.5V	2.8V
VREF	Input reference voltage (VREF = 0.5 * VDDR for SSTL2, VREF = 0.45 * VDDR for SSTL3)	1.15V	1.25V	1.35V
VTT	Termination voltage	VREF -40mV	VREF	VREF +40mV
VIH(dc)	DCinput logic HIGH	VREF +180mV	--	VDDR +300mV
VIL(dc)	DC input logic LOW	- 300mV	--	VREF -180mV
VIH(ac)	ACinput logicHIGH	VREF +350mV	--	--

Table 5-8 Memory Interface Electrical Characteristics SSTL (Continued)

Symbol	Parameter	SSTL-2		
		Min	Norm	Max
VIL(ac)	AC input logic LOW	--	--	VREF -350mV
Delta Vout1 (7.6 mAx50 Ohm)		380mV	380mV	380mV
Delta Vout2 (0.38V+0.38V/2)		570mV	570mV	570mV
Output High Driver (worst case)	Vmin at VIN (1.11V+350mV)	1.47V	1.47V	1.47V
	Vmin at VOUT (1.11V + 0.57V)	1.69V	1.69V	1.69V
	Imin output (0.57V+0.38V)/25 Ohm	-7.6mA	-7.6mA	-7.6mA
	Max.ON resistor Ohm (2.5V-1.25V-0.57V)/7.6mA	80.26	89.47	98.68
Output Low Driver (worst case)	Vmax at VIN (1.11V-0.35V)	0.77V	0.90V	1.03V
	Vmax at VOUT (1.11V-0.57V)	0.55V	0.68V	0.81V
	Imin output	7.6mA	7.6mA	7.6mA
	Max.ON resistor Ohm	72.37	89.47	106.58

Notes:
- Peak to peak ac noise on VREF may not exceed +/- 25mV (+/-0.2% VREF).
- VTT of transmitting device must track VREF of receiving device.
- The 1V/ns input signal minimum slew rate is to be maintained.
- In cases where the differential signaling interface on the memory is not used VREF should be connected to the memory IO's VDDR (3.3 or 2.5 V).

5.7 DAC Characteristics

Table 5-9 DAC Characteristics

Parameter	Min	Typ	Max	Notes
Resolution	10 bits	-	-	a
Vo (max) - Maximum Output Voltage	-	0.700 V	0.770 V	a
Io (max) - Maximum Output Current	-	60 mA	-	a
Full Scale Error	- 5%	-	+10%	b,c
DAC to DAC Correlation	-1%	-	+1%	a,d
Integral Linearity	-2 LSB	-	+2 LSB	a,e
Rise Time (10% to 90%)	-	-	3 ns	a,f
Full Scale Settling Time	-	< 8ns	-	a,g,h
Glitch Energy	-	60 pV-s	-	a,h
Monotonicity	-	-	-	i

Notes:
a: Tested over the operating temperature range, at nominal supply voltage, with an Iref of -3.04mA. (Iref is the level of the current flowing out of the Rset resistor.)
b: Tested over the operating temperature range, at reduced supply voltage, with an Iref of -3.04mA.
c: Full scale error from the value predicted by the design equations.
d: About the mid point of the distribution of the three DACs measured at full scale deflection.
e: Linearity measured from the best fit line through the DAC characteristics. Monotonicity guaranteed.
f: Load = 37.5Ω + 20 pF with Iref = -3.04 mA.
g: From a 2% change in the output voltage until settling to within 2% of the final value.
h: This parameter is sampled, not 100% tested.
i: Monotonicity is guaranteed.

5.7.1 Calculating RSET (CRT DAC Interface) and R2SET Resistances (TV DAC Interface)

A precision resistor (with 1% of nominal) is placed between RSET (or R2SET) and analog ground AVSS (or A2VSS) to set the full-scale DAC current. This required resistor value can be calculated using the formula below.

$$\mathbf{RSET\ (\Omega) = (G \times V_{REF} \times \alpha \times \beta) / I_{OUT}}$$

where:

G =1023/N is the idealized 10-bit gain constant (N is the number of current sources for a particular display mode, see *Table 5-10* and *Table 5-11*)

$\mathbf{V_{REF}}$ is the idealized reference voltage (0.75V for CRT and 1.18V for TV)

α is the systematic **composite** skew on idealized V_{REF} and gain constant, which can be assumed to be 1

β is a scaling factor (1 for RGB, 0.7296 for PAL, and 0.7727 for NTSC)

$\mathbf{I_{OUT} = V_{WHITE} / Z_{EFF}}$ is the required DAC full-scale current. ($\mathbf{Z_{EFF}}$ = 37.5 Ω (double terminated 75 Ω, see figure below))

For values of $\mathbf{V_{REF}}$, $\mathbf{V_{WHITE}}$ and $\mathbf{I_{OUT}}$, see *Table 5-10 and Table 5-11.*

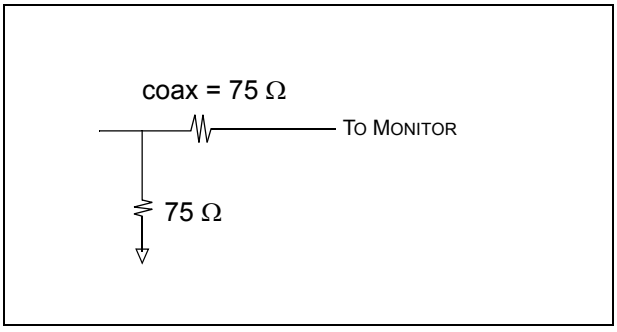

Figure 5-1. Double Termination

Defining RSET (or R2SET) in this fashion allows for a one-time compensation for the systematic skew due to shifts on both V_{REF} and the gain constant on the output white level by adjustment of α.

Table 5-10 CRT DAC (DAC1) Electrical Parameters

Mode	V_{REF} (V)	V_{white} (V)			I_{out} (mA)			N (# of Current Sources)
		Min.	Typ.	Max.	Min.	Typ.	Max.	
PS-2	0.75	0.665	0.700	0.770	-5%	18.66	+10%	82

Calculating RSET for PS-2 Case (N=82)

$$\mathbf{RSET\ (\Omega) = (1023/82 \times V_{REF} \times \alpha \times \beta) / I_{OUT}}$$
$$\mathbf{= (12.47 \times 0.75 \times 1 \times 1) / 0.0186}$$
$$\mathbf{= 503\Omega}$$

However the closest standard 1% tolerant resistor is **499Ω**.

Table 5-11 TV DAC (DAC2) Electrical Parameters

Mode	V_{REF} (V)	V_{white} (V)			I_{out} (mA)			N (# of Current Sources)
		Min.	Typ.	Max.	Min.	Typ.	Max.	
PS-2	1.00	0.665	0.700	0.770	-5%	18.66	+10%	76
PAL	1.00	0.918	1.020	1.122	-10%	27.20	+10%	38
NTSC	1.00	0.918	1.020	1.122	-10%	27.20	+10%	40

Calculating R2SET

Example 1: PS-2 Case (N=76)

$$R2SET\ (\Omega) = (1023/76 \times V_{REF} \times \alpha \times \beta) / I_{OUT}$$
$$= (13.46 \times 1 \times 1 \times 1) / 0.0187$$
$$= 719.81\Omega$$

However closest standard 1% tolerant resistor is **715**Ω.

Example 2: PAL Case (N=38)

$$R2SET\ (\Omega) = (1023/38 \times V_{REF} \times \alpha \times \beta) / I_{OUT}$$
$$= (26.92 \times 1 \times 1 \times 0.7296) / 0.0272$$
$$= 722\Omega$$

However closest standard 1% tolerant resistor is **715**Ω.

Example 3: NTSC Case (N=40)

$$R2SET\ (\Omega) = (1023/40 \times V_{REF} \times \alpha \times \beta) / I_{OUT}$$
$$= (25.57 \times 1 \times 1 \times 0.7727) / 0.0272$$
$$= 726.39\Omega$$

However closest standard 1% tolerant resistor is **715**Ω.

5.7.2 Analog Video Levels

Conceptually, each 10-bit DAC can be viewed as two current sources connected in parallel. Each current source is controlled independently as shown below.

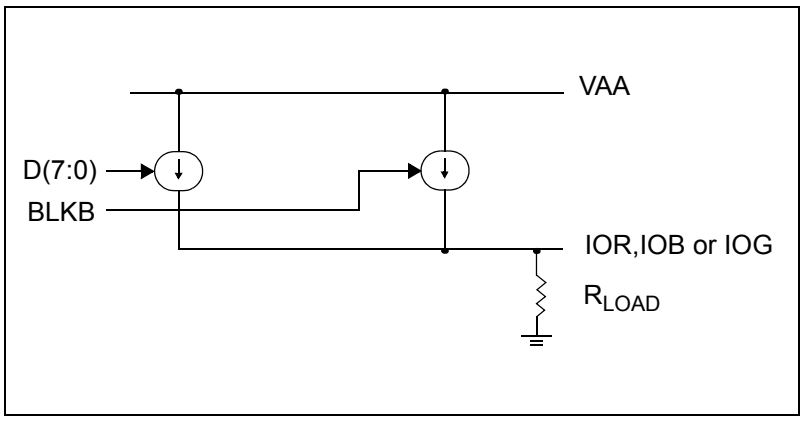

Figure 5-2. Analog Output (DAC)

The following diagrams show video levels for PS/2, NTSC and PAL.

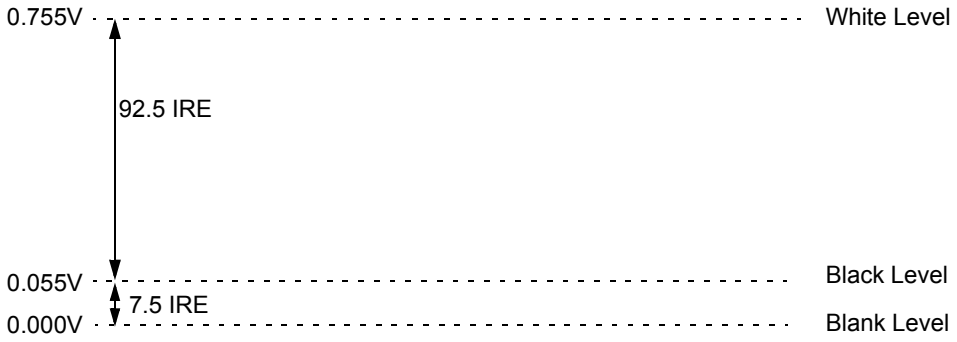

Figure 5-3. PS/2 Video Levels

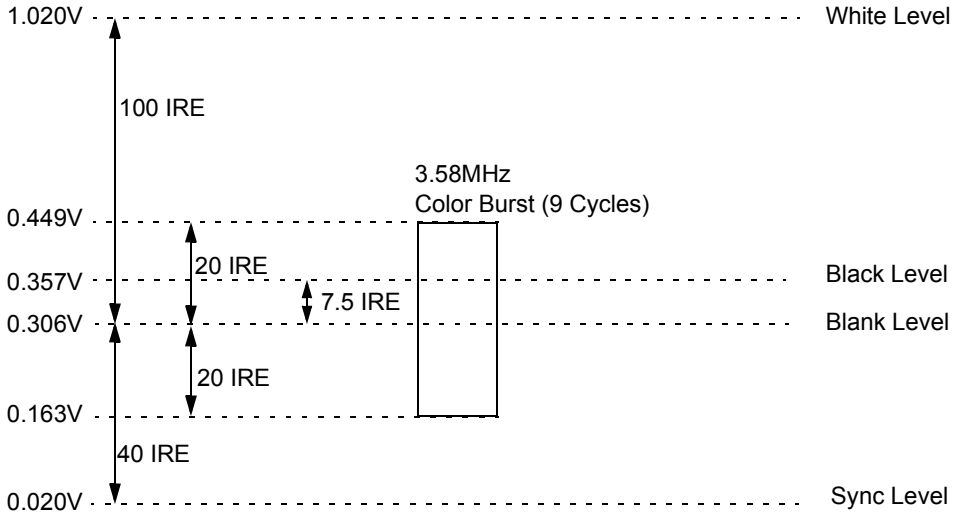

Figure 5-4. NTSC Video Levels

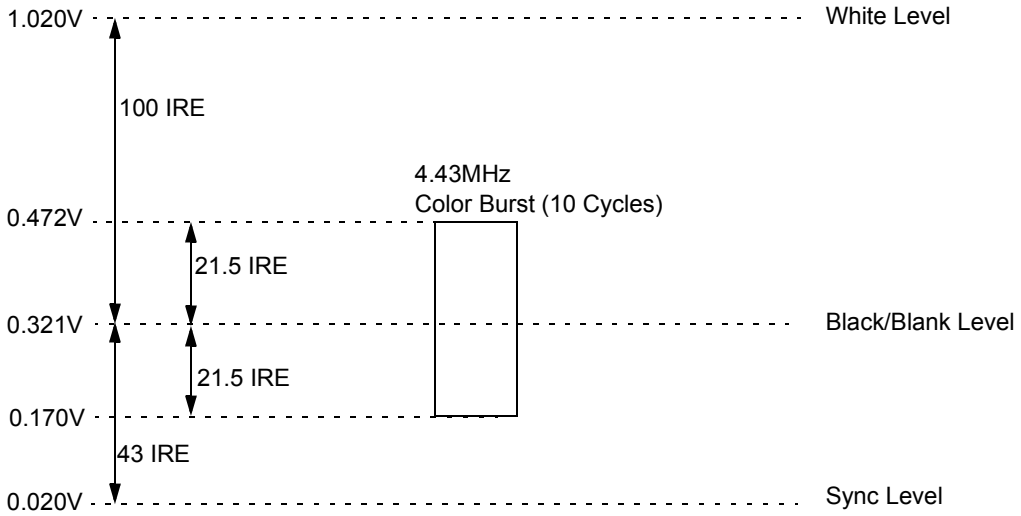

Figure 5-5. PAL Video Levels

Chapter 6
Thermal Data

6.1 Thermal Equations

The thermal property of an IC package can be characterized by the important parameter θJA (junction-to-ambient thermal resistance) defined by:

$$\theta_{JA} = (T_J - T_A) / P$$

Where:

T_J is the chip junction temperature;

T_A is the ambient temperature;

P is the power dissipation

Or by θCA (case-to-ambient thermal resistance), defined by:

$$\theta_{CA} = (T_C - T_A) / P$$

Where T_C is the case temperature.

In addition, θ**JA** and θ**CA** are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

Where θ**JC** is junction-to-case thermal resistance.

With the above equations, important thermal parameters such as maximum ambient temperature and maximum case temperature can be calculated from given values of maximum power dissipation **Pmax**, θ**JC**, maximum allowed junction temperature **TJmax**, and air flow data.

6.1.1 Maximum Ambient Temperature and Case Temperature

The RADEON 9800 chip has the following thermal characteristics:

- Maximum absolute rated junction temperature: TJmax = 125°C
- Maximum operating power dissipation: Pmax = 48.60W
- Maximum case temperature: TCmax = 125°C
- Junction to case thermal resistance: θJC ~ 0°C/W
  Note: Since RADEON 9800 is a flip chip package, where the case is the back side of the bulk silicon, θ**JC** is close to zero. This means that the junction temp will be largely determined by the thermal characteristics (i.e., θ**JA**) of the external heat sink provided by the customer.

6.1.2 Heat Sink Selection

Heat sink and fan characteristics should be selected to ensure that maximum case temperature does not exceed 125 °C. Refer to heat sink manufacturers' data and application notes for selecting the appropriate heat sink.

However, the heat sink should be selected such that the ASIC case temperature is well below the TCmax of 125°C for good reliability. For example, considering the ambient operating temperature of 50°C and to obtain an ASIC case temperature of about 110°C, select a heatsink with a thermal impedance of 3.06°C/W to dissipate 48.60W of power.

6.2 R360/R350 Power Dissipation

The following are the average and maximum power dissipation values for the R360/R350. Three different test modes were used: Static-Windows, Winbench 99, and 3D Mark 2001.

Table 6-1 Power Dissipation

	1600x1200, 32bpp, 70Hz Mode Static-Windows Test		1024x768, 32bpp, 75Hz Mode Winbench 99 Test		1600x1200, 32bpp, 60Hz Mode 3D Mark 2001 Test	
	Average	**Maximum**	**Average**	**Maximum**	**Average**	**Maximum**
RADEON 9800 XT, 256MB DDR Hynix. Core Voltage: 1.77V. VDDQ Voltage: 1.5V.						
Current (mA) VDDQ Power on AGP bus connector	28.26				28.44	30.58
Current (mA) 12V Power on AGP/PCI bus connector	164.80				178.98	220.83
Current (mA) 5V Power on AGP/PCI bus connector	532.84				776.87	1529.60
Current (mA) 3.3V Power on AGP bus connector	1437.90				2151.61	4335.09
Board AGP Bus Power (W)	9.38				13.05	23.53
Current (mA) with external power connector +5V	2459.12				3008.75	3989.07
Current (mA) with external power connector +12V	1413.11				1727.09	2459.91
Total Board Power (W)	38.43				48.51	71.57
RADEON 9800 PRO DDR-1, 128MB DDR Samsung. Core Voltage: 1.70V. VDDQ Voltage: 1.5V. (approximate values)						
Current (mA) VDDQ Power on AGP bus connector	28.34		28.48	30.63	28.55	30.75
Current (mA) 12V Power on AGP/PCI bus connector	153.56		153.99	155.22	154.58	156.82
Current (mA) 5V Power on AGP/PCI bus connector	513.12		505.64	659.63	751.31	1498.04
Current (mA) 3.3V Power on AGP bus connector	3169.89		3209.33	3922.33	3785.19	5353.00
Board AGP Bus Power (W)	14.73		14.82	17.22	17.86	26.14
Current (mA) with external power connector +5V	3481.46		3523.10	4349.18	4187.48	5959.63
Current (mA) with external power connector +12V	286.45		268.46	538.83	499.99	1149.07
Total Board Power (W)	35.27		35.35	43.53	44.34	68.09

Table 6-1 Power Dissipation (Continued)

	1600x1200, 32bpp, 70Hz Mode Static-Windows Test		1024x768, 32bpp, 75Hz Mode Winbench 99 Test		1600x1200, 32bpp, 60Hz Mode 3D Mark 2001 Test	
	Average	**Maximum**	**Average**	**Maximum**	**Average**	**Maximum**
RADEON 9800 PRO DDR-2, 256MB DDR Samsung. Core Voltage: 1.62V. VDDQ Voltage: 1.5V.						
Current (mA) VDDQ Power on AGP bus connector	28.76		28.93	30.66	28.92	31.31
Current (mA) 12V Power on AGP/PCI bus connector	130.02		132.39	133.45	132.59	133.97
Current (mA) 5V Power on AGP/PCI bus connector	1597.94		1620.33	1696.33	1728.38	2102.39
Current (mA) 3.3V Power on AGP bus connector	2713.84		2812.69	3142.17	3358.48	4660.41
Board AGP Bus Power (W)	18.30		18.75	19.96	21.01	26.83
Current (mA) with external power connector +5V	2947.02		3078.21	3524.42	3658.35	5187.53
Current (mA) with external power connector +12V	555.27		534.77	683.87	746.30	1318.38
Total Board Power (W)	39.47		40.31	43.56	47.90	67.13
RADEON 9800, 128MB DDR Samsung. Core Voltage: 1.70V. VDDQ Voltage: 1.5V.						
Current (mA) VDDQ Power on AGP bus connector	28.42		28.53	30.99	28.60	30.71
Current (mA) 12V Power on AGP/PCI bus connector	153.49		153.93	154.82	154.34	156.57
Current (mA) 5V Power on AGP/PCI bus connector	518.49		512.28	639.54	771.28	1497.51
Current (mA) 3.3V Power on AGP bus connector	2902.60		2909.99	3277.02	3454.71	4731.73
Board AGP Bus Power (W)	13.92		13.91	15.10	16.93	24.23
Current (mA) with external power connector +5V	3176.92		3187.58	3675.46	3831.32	5311.69
Current (mA) with external power connector +12V	288.52		273.30	488.06	509.05	1095.91
Total Board Power (W)	32.57		32.44	35.88	41.30	62.18
RADEON 9800 SE, 128MB DDR Samsung. Core Voltage: 1.52V. VDDQ Voltage: 1.5V.						
Current (mA) VDDQ Power on AGP bus connector	20.79		20.97	23.23	21.08	23.29
Current (mA) 12V Power on AGP/PCI bus connector	109.16		109.17	110.17	109.83	111.22

Table 6-1 Power Dissipation (Continued)

	1600x1200, 32bpp, 70Hz Mode Static-Windows Test		1024x768, 32bpp, 75Hz Mode Winbench 99 Test		1600x1200, 32bpp, 60Hz Mode 3D Mark 2001 Test	
	Average	**Maximum**	**Average**	**Maximum**	**Average**	**Maximum**
Current (mA) 5V Power on AGP/PCI bus connector	531.60		531.22	963.34	741.68	1178.56
Current (mA) 3.3V Power on AGP bus connector	2546.95		2657.20	3629.64	3459.75	4790.64
Board AGP Bus Power (W)	12.28		12.63	17.23	16.24	22.20
Current (mA) with external power connector +5V	2475.39		2462.87	2645.41	2672.40	3152.92
Current (mA) with external power connector +12V	281.01		273.67	596.94	414.79	676.76
Total Board Power (W)	27.87		28.08	33.34	34.39	45.54

6.3 ASIC Case Temperature and Junction Temperature

The following are the ASIC case and junction temperatures for the R360/R350.

Table 6-2 ASIC Case Temperature and Junction Temperature

Parameter	1600x1200, 32bpp, 70Hz Mode Static-Windows Test		1024x768, 32bpp, 75Hz Mode Winbench 99 Test		1600x1200, 32bpp, 60Hz Mode 3D Mark 2001 Test	
	Average	Maximum	Average	Maximum	Average	Maximum
RADEON 9800 XT Core Voltage: 1.77V. VDDQ Voltage: 1.5V. With Heatscape Active Heat Sink. (approximate values)						
ASIC Case Temperature at Room Temperature Ambient (°C)						70* (best case scenario, see note)
ASIC Case Temperature at 55C Ambient (°C)						
Junction Temperature at 55C Ambient (°C)						
* Note that this value is obtained using a very efficient heatsink such as the Heatscape heat sink. If a low cost and less efficient heatsink is used instead, this temperature may rise up to 85C.						
RADEON 9800 PRO DDR-1 Core Voltage: 1.70V. VDDQ Voltage: 1.5V. With Active Heat Sink.						
ASIC Case Temperature at Room Temperature Ambient (°C)	63.9		65.7	67.2	80.2	84.2
ASIC Case Temperature at 55C Ambient (°C)						109.3
Junction Temperature at 55C Ambient (°C)						111.3
RADEON 9800 PRO DDR-2 Core Voltage: 1.62V. VDDQ Voltage: 1.5V. With Active Heat Sink.						
ASIC Case Temperature at Room Temperature Ambient (°C)						84.5
ASIC Case Temperature at 55C Ambient (°C)						109.6
Junction Temperature at 55C Ambient (°C)						111.6
RADEON 9800 Core Voltage: 1.70V. VDDQ Voltage: 1.5V. With Active Heat Sink.						
ASIC Case Temperature at Room Temperature Ambient (°C)	63.1		63.3	64.2	75.1	79.1
ASIC Case Temperature at 55C Ambient (°C)						
Junction Temperature at 55C Ambient (°C)						
RADEON 9800 SE Core Voltage: 1.52V. VDDQ Voltage: 1.5V. With Active Heat Sink.						
ASIC Case Temperature at Room Temperature Ambient (°C)						87.6
ASIC Case Temperature at 55C Ambient (°C)						112.7
Junction Temperature at 55C Ambient (°C)						114.7

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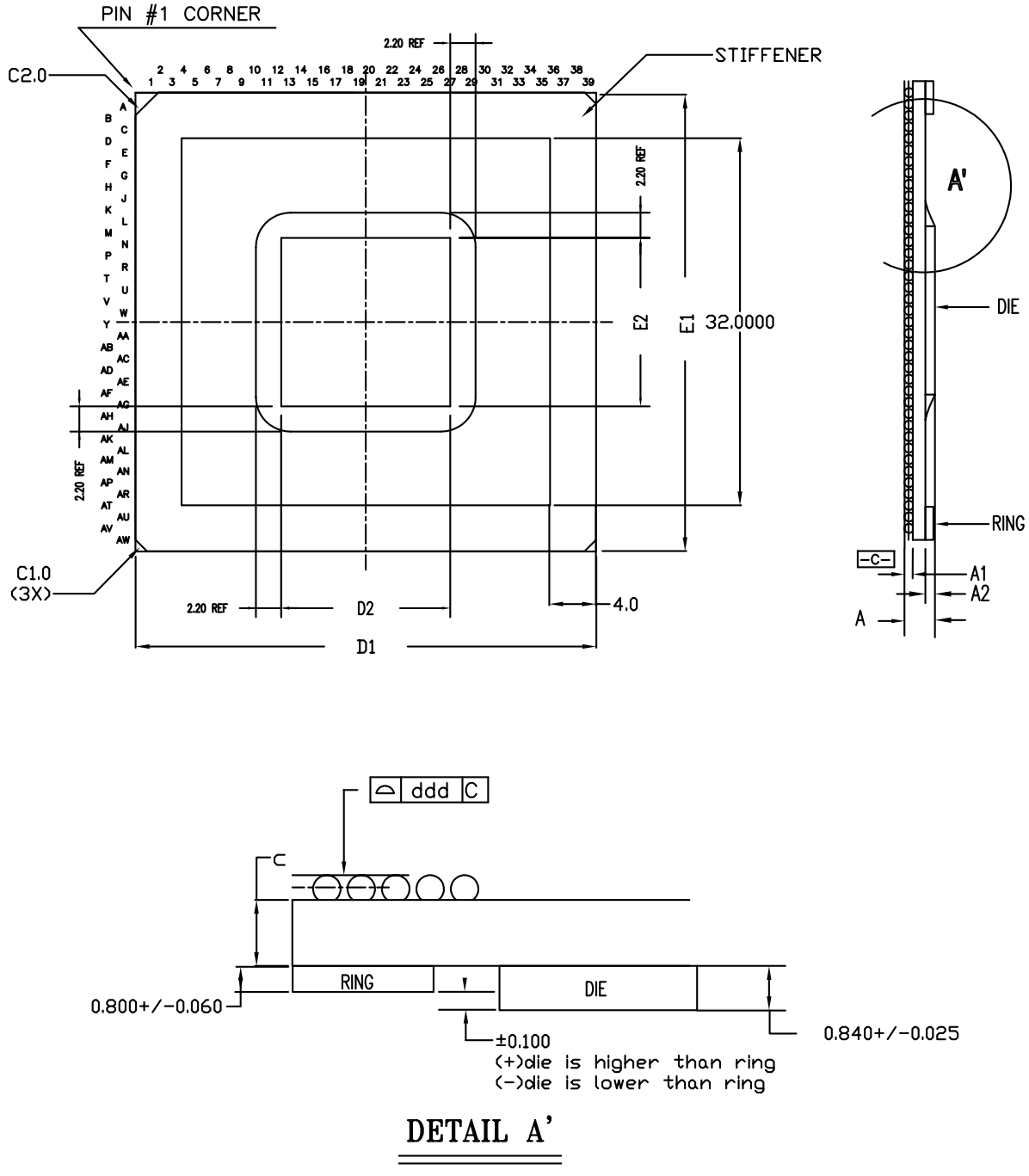

Figure 7-1. RADEON 9800 Package Outline - Top and Side View

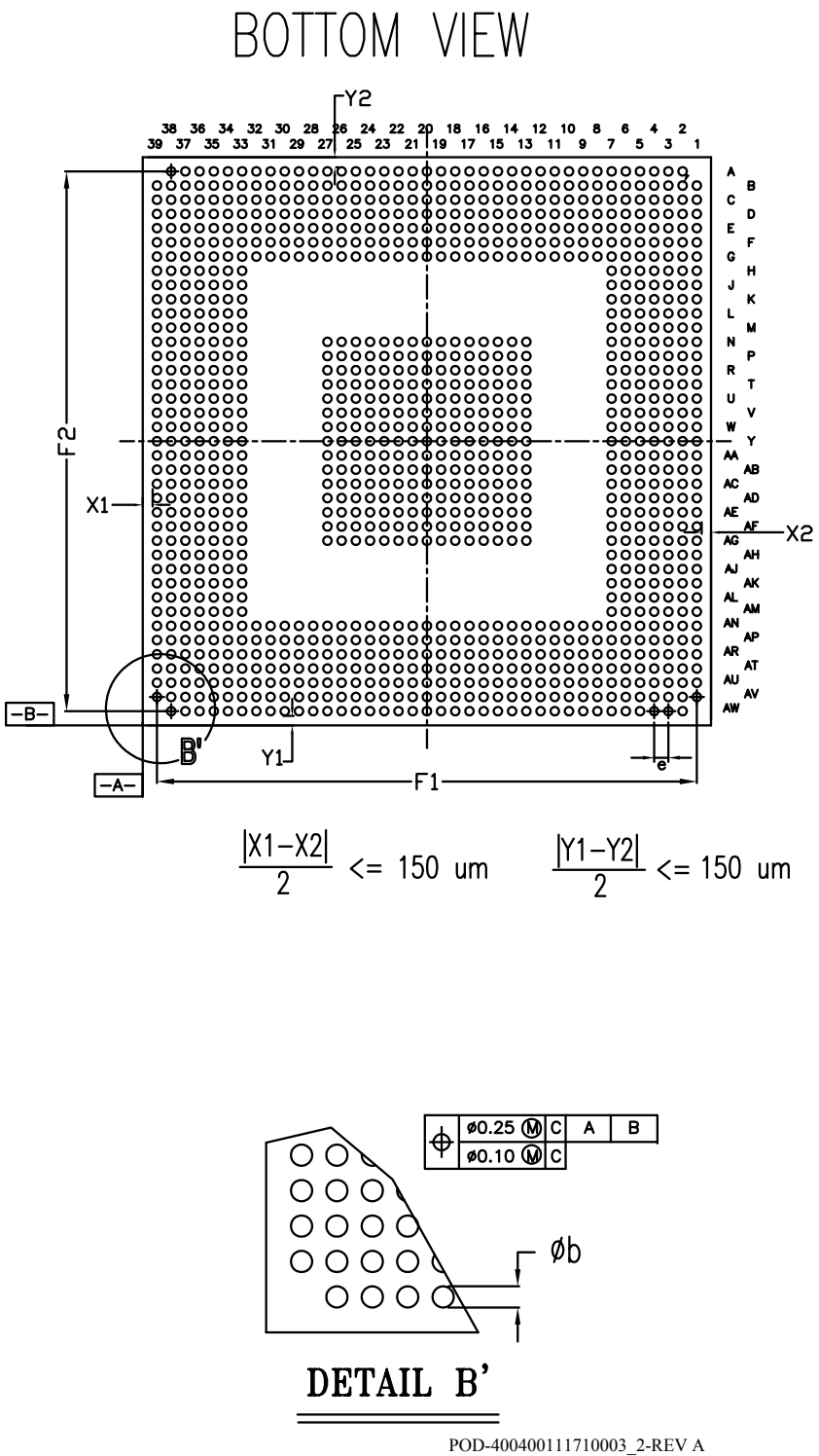

Figure 7-2. RADEON 9800 Package Outline - Bottom View

Table 7-1 RADEON 9800 Physical Dimensions

Symbol	Min (mm)	Normal (mm)	Max (mm)
c	0.91	1.06	1.21
A	2.05	2.36	2.68
A1	0.40	0.50	0.60
A2	0.74	0.80	0.87
ϕb	0.50	0.60	0.70
D1	39.90	40.00	40.10
D2		14.68	
E1	39.90	40.00	40.10
E2	14.68 REF		
F1	-	38.00	-
F2	-	38.00	-
e	-	1.00	-
ddd	-	-	0.20

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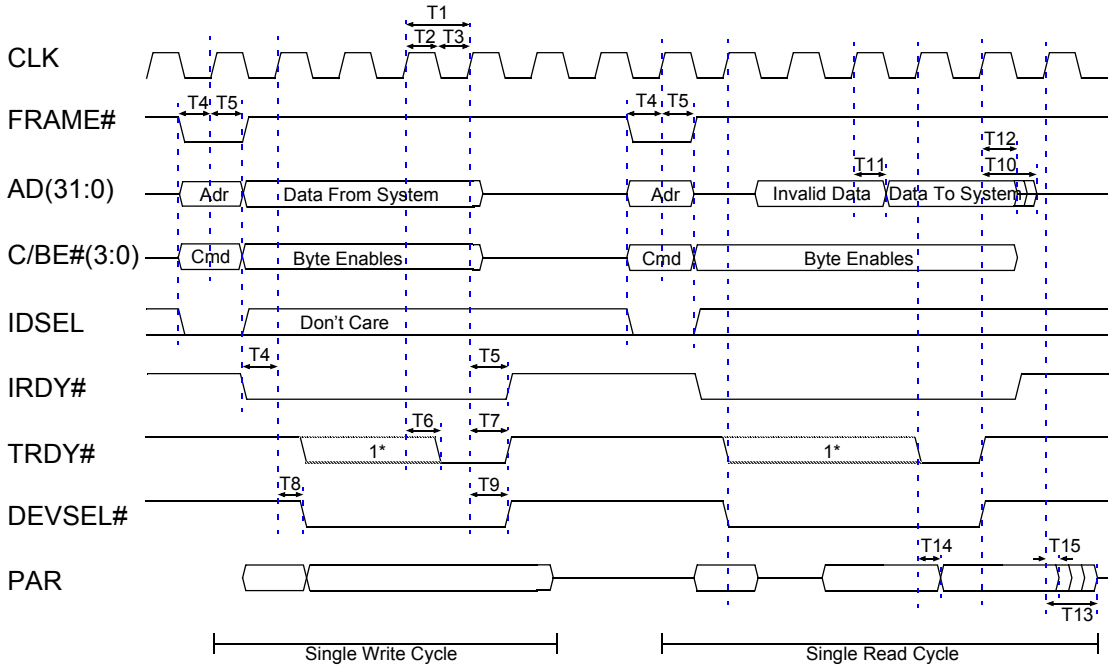
Chapter 8
Timing Specifications

This chapter describes bus and memory timing specifications of the RADEON 9800. To link to a topic of interest, use the following list of linked cross references:

8.1 Bus Timing

8.1.1 Single Read/Write Cycle Timing - PCI Bus



1* The minimum number of clocks from FRAME# active to TRDY# active is programmable.

Figure 8-1. Single Read/Write Cycle Timing - PCI Bus

8.1.2 Disconnect On Burst Cycle - PCI Bus

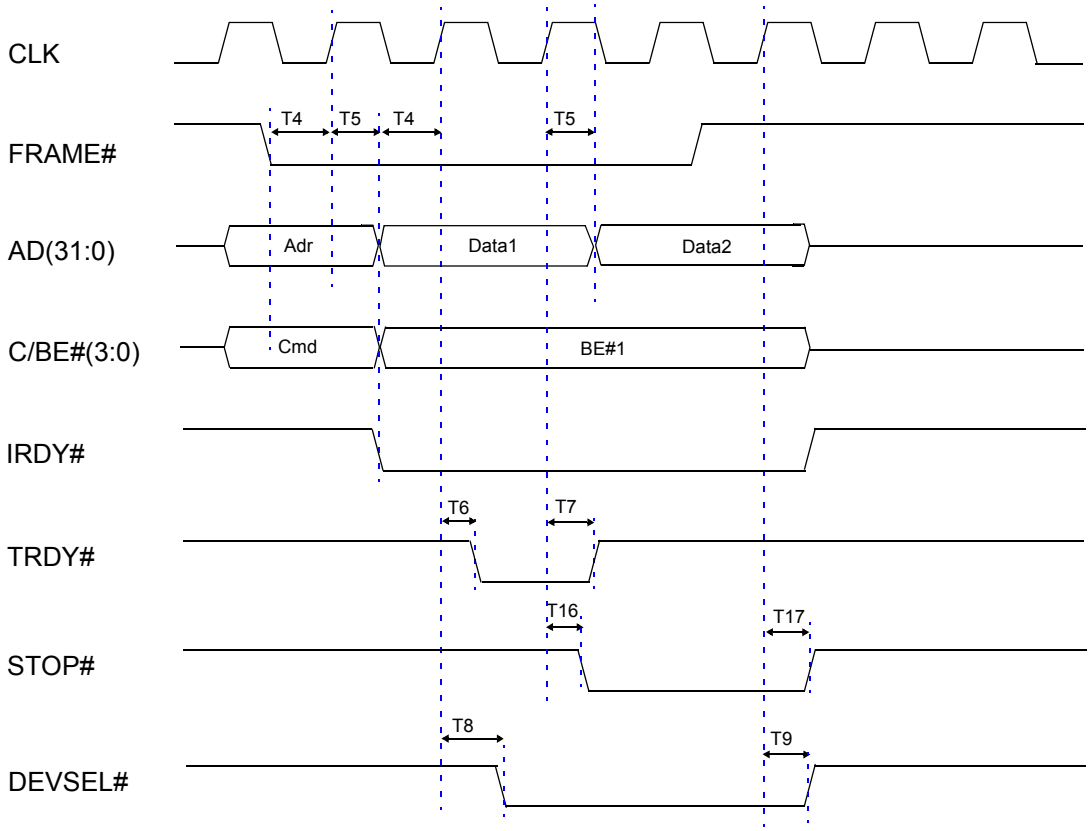


Figure 8-2. Disconnect On Burst Cycle - PCI Bus

8.1.3 Burst Access Timing - PCI Bus

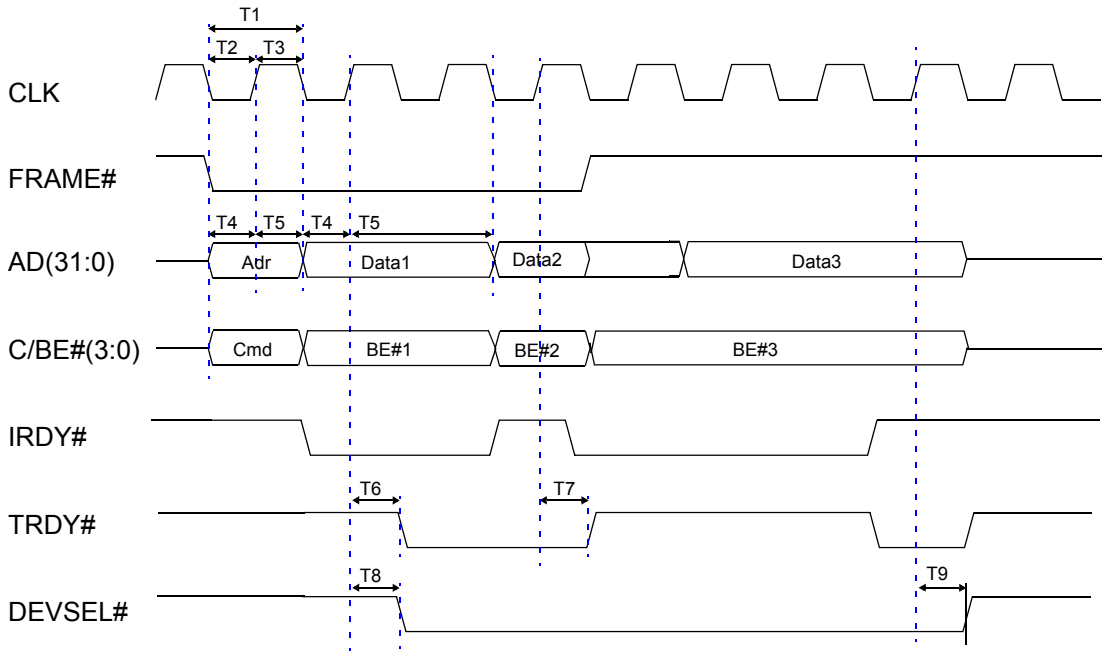


Figure 8-3. Burst Access Timing - PCI Bus

8.1.4 PCI Bus Master Operation

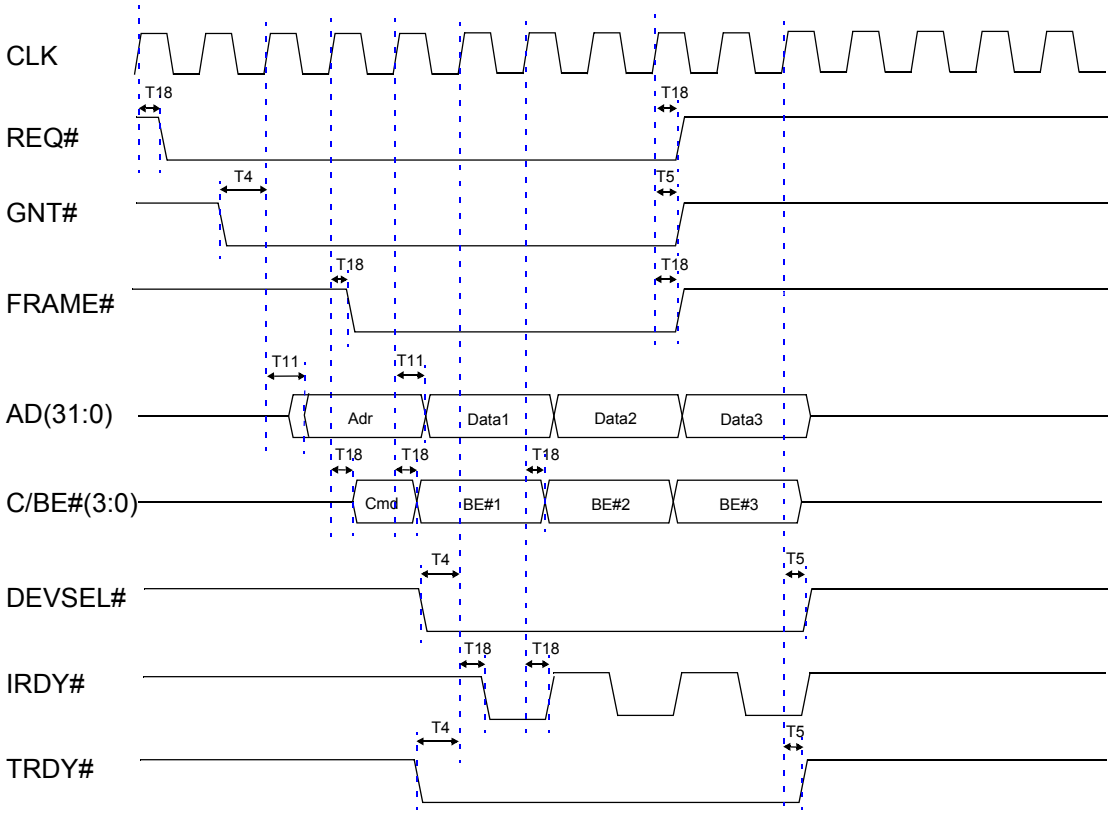


Figure 8-4. PCI Bus Master Operation

Table 8-1 PCI Bus Interface Timing Parameters

Symbol	Description	Min.(ns)	Max.(ns)
T1	Bus Clock Period	30	-
T2	Bus Clock High Time	12	-
T3	Bus Clock Low Time	12	-
T4	Bus Input Signal Setup to CLK[a]	7	-
T5	Bus Input Signal Hold from CLK[a]	0	-
T6	CLK to TRDY# active	2	11
T7	CLK to TRDY# inactive	2	11
T8	CLK to DEVSEL# active	2	11
T9	CLK to DEVSEL# inactive	2	11
T10	CLK to data output tri-state	2	20
T11	CLK to data output valid delay (data stepping buffer)	2	20
T12	CLK to data output invalid delay	2	-
T13	CLK to PAR tri-state	2	20
T14	CLK to PAR valid delay (data stepping buffer)	2	20
T15	CLK to PAR invalid delay	2	-
T16	CLK to STOP# active delay	2	11
T17	CLK to STOP# inactive delay	2	11
T18	CLK to signal valid delay	2	11

a. Bus input signals include FRAME#, AD(31-0), IDSEL, IRDY#, TRDY#, GNT#, DEVSEL#.

8.1.5 AGP 1X / 2X Timing

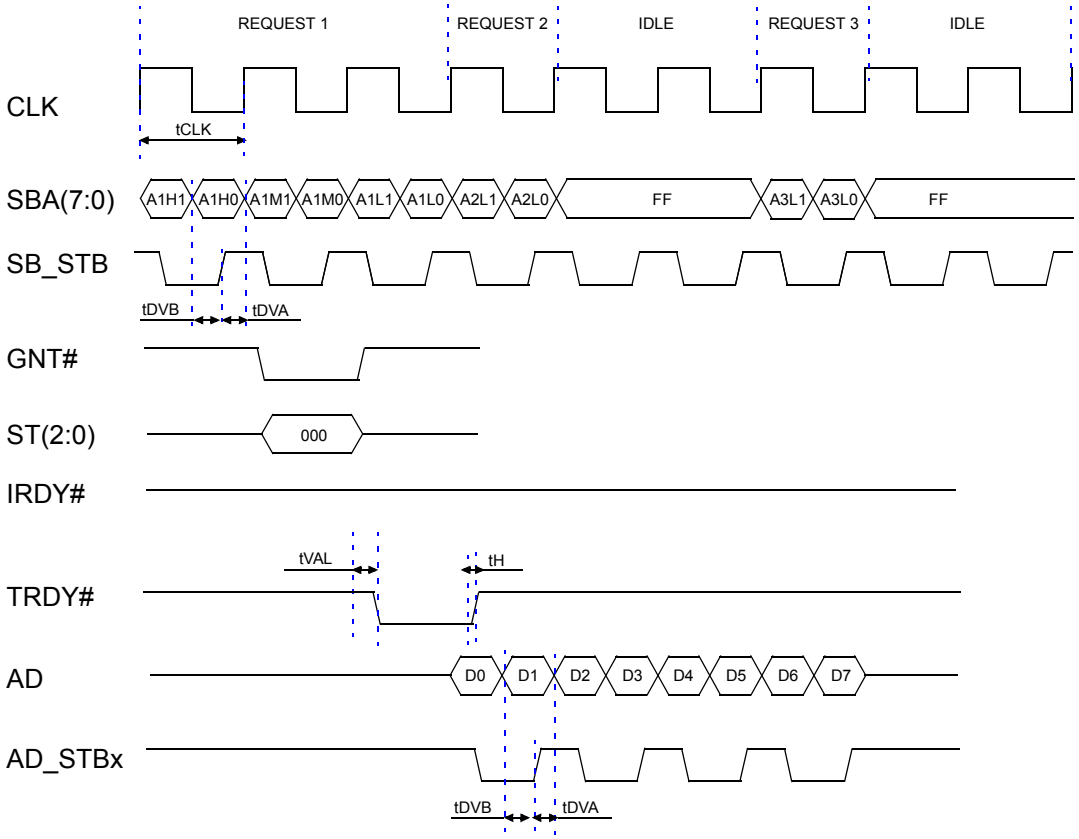


Figure 8-5. AGP 2X Read Request with Return Data (4Qw)

Table 8-2 AGP 2X Timing Parameters

Symbol	Description	Min.(ns)	Max.(ns)
tCLK	Clock	-	15
tDVB	Data valid before	1.7	
tDVA	Data valid after	1.7	-
tVAL	CLK to control signal and Data valid delay	1	5.5
tH	Control signals hold time to CLK	0	-

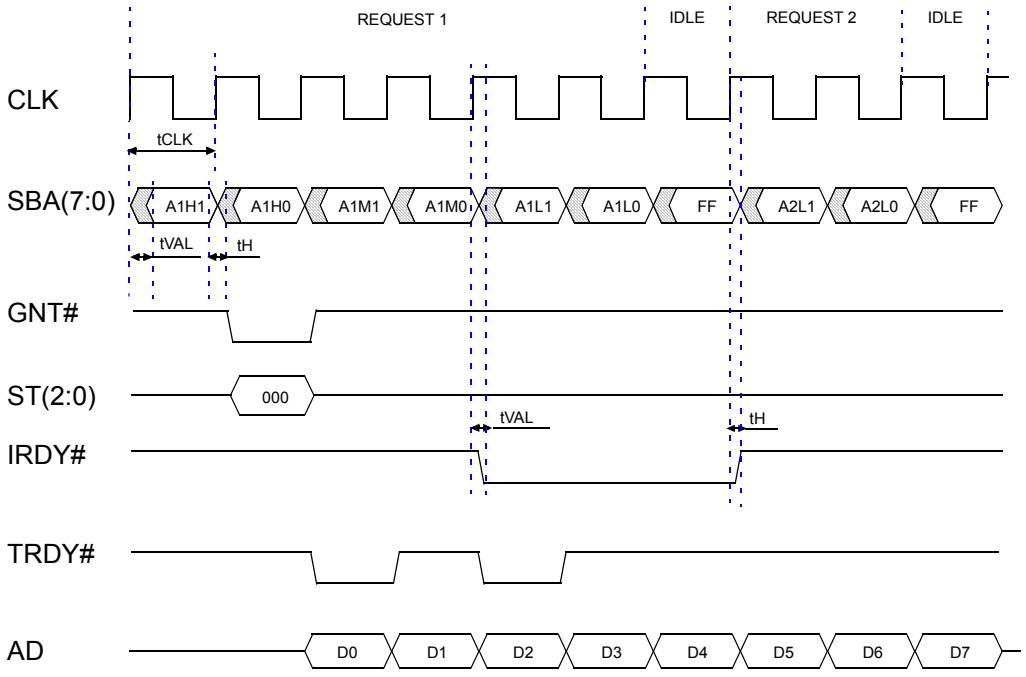


Figure 8-6. AGP 1X Read Request with Return Data (4Qw)

Table 8-3 AGP 1X Timing Parameters

Symbol	Description	Min.(ns)	Max.(ns)
tVAL	CLK to control signal and Data valid delay	1	5.5
tH	Control signals hold time to CLK	0	-

8.1.6 AGP 4X Timing

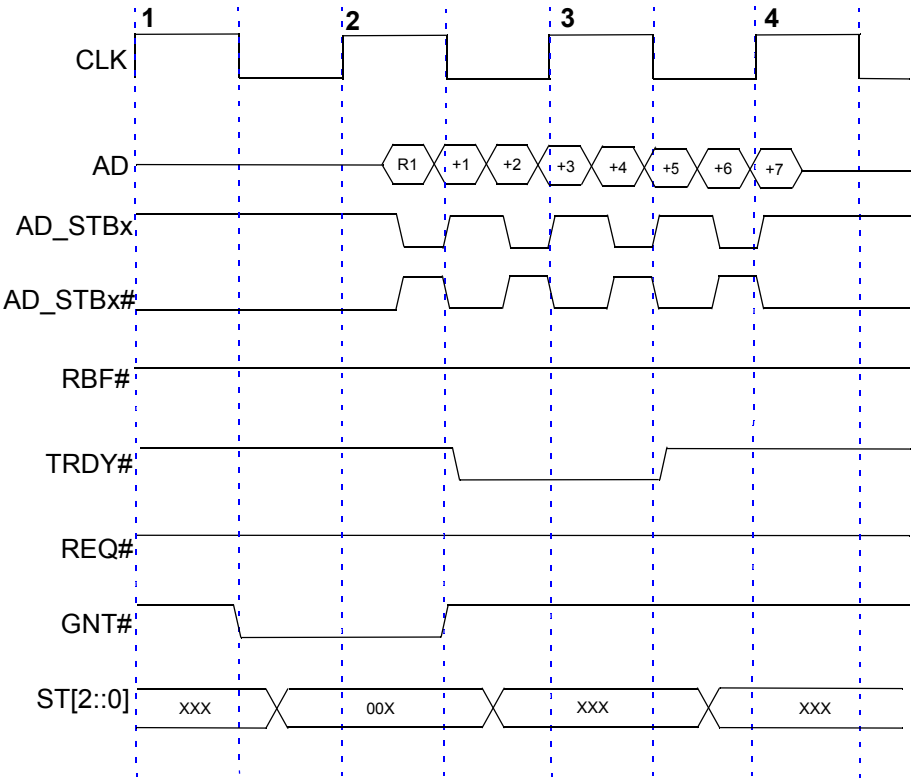


Figure 8-7. AGP 4X Read Data - No Delay

Table 8-4 AGP 4X AC Timing Parameters (Transmitter Output Signals)

Symbol	Description	Min	Max	Units
t_{TSf}	CLK to first transmit strobe transaction	1.9	8	ns
t_{TSr}	CLK to 4th transmit strobe transaction		20	ns
t_{Dvb}	Data valid before strobe	0.95		ns
t_{Dva}	Data valid after strobe	1.15		ns
t_{ONd}	Float to active delay	-1	7	ns
t_{OFFd}	Active to float delay	1	14	ns
t_{ONs}	Strobe active to first strobe float delay	4	9	ns
t_{OFFs}	Last strobe edge to strobe float delay	4	9	ns

Table 8-5 AGP 4X AC Timing Parameters (Receiver Input Signals)

Symbol	Description	Min	Max	Units
t_{RSsu}	Receive strobe setup time to CLK	6		ns
t_{SRh}	Receive strobe hold time from CLK	0.5		ns
t_{Dsu}	Data to strobe setup time	0.4		ns
t_{Dh}	Strobe to data hold time	0.7		ns

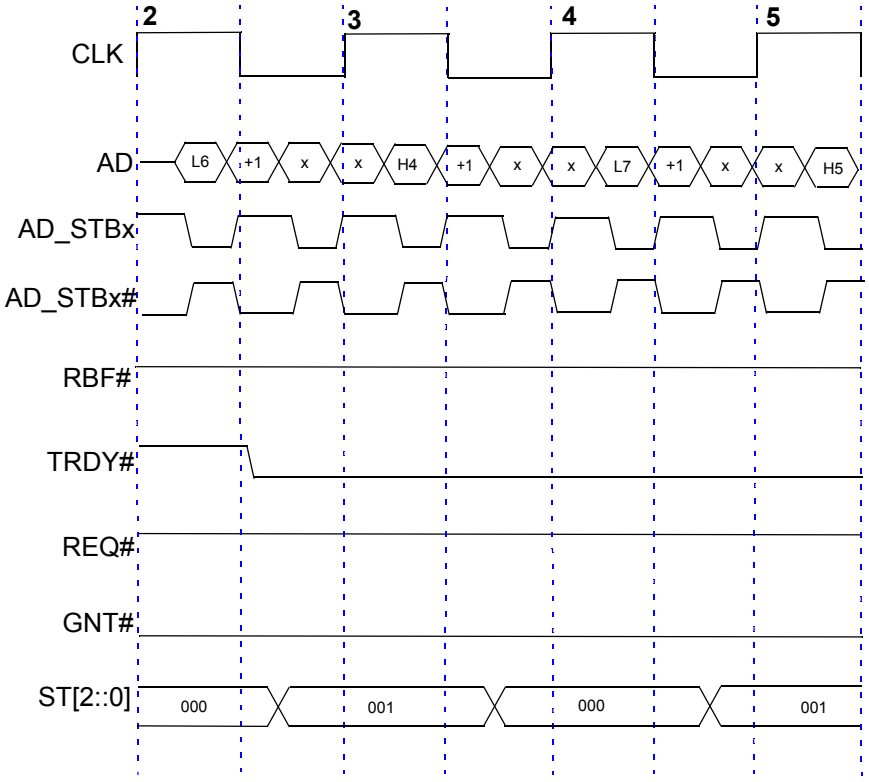


Figure 8-8. AGP 4X Back-to-back Read Data - No Delay

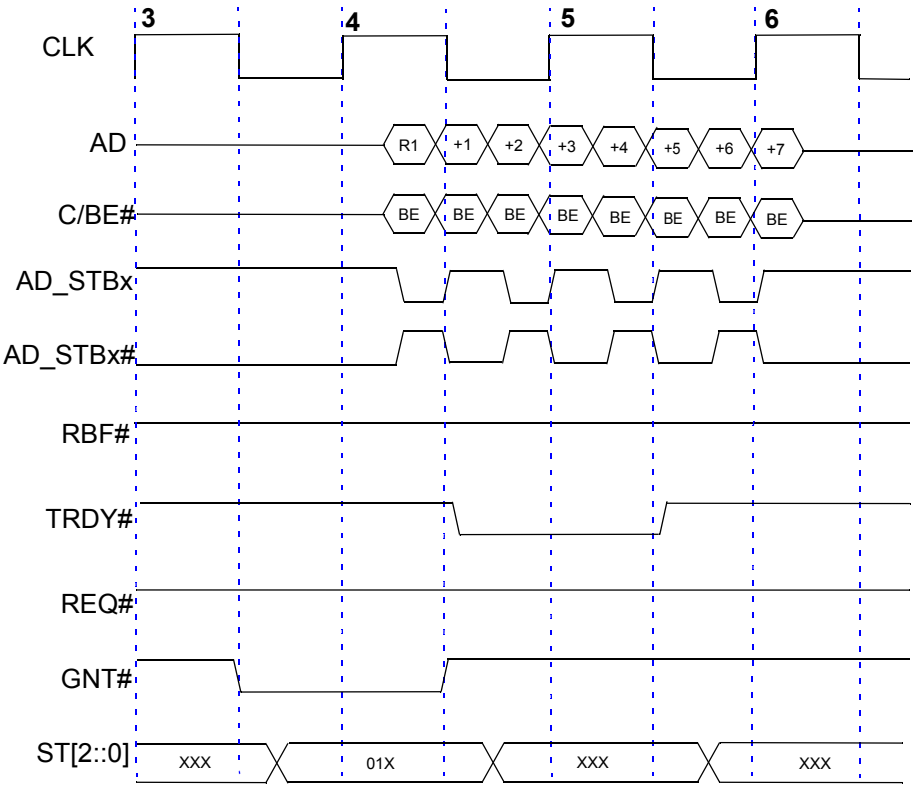


Figure 8-9. AGP 4X Basic Write - No Delay

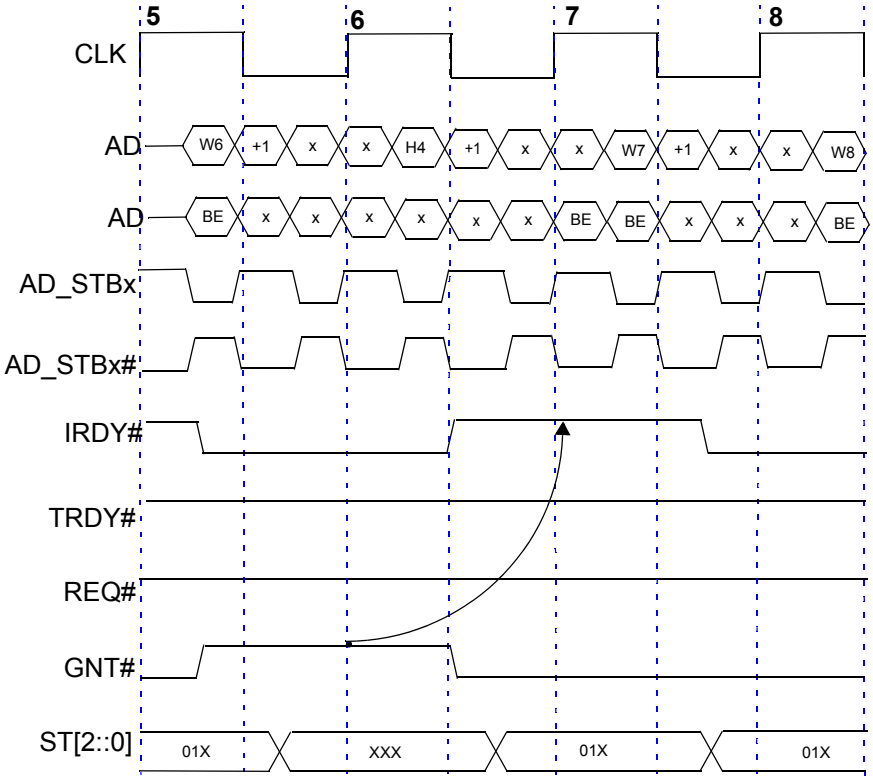


Figure 8-10. AGP 4X Quad Word Writes - No Delay

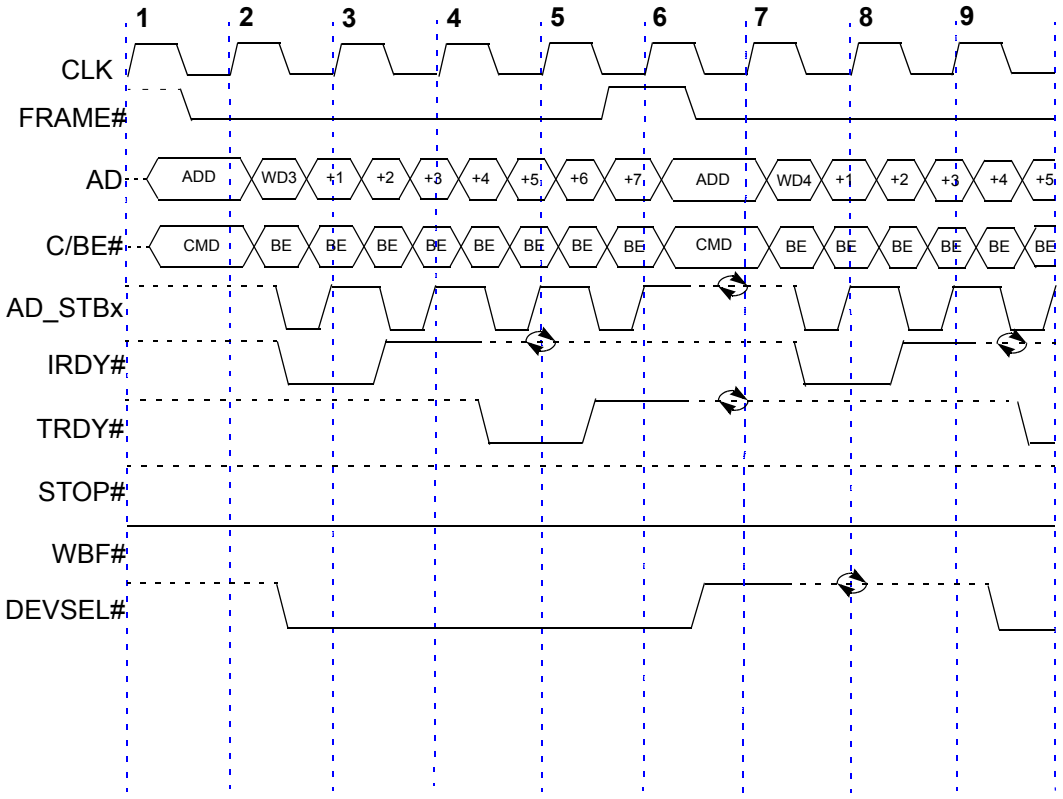


Figure 8-11. Fast Back-to-Back Transaction

8.1.7 AGP 8X Timing

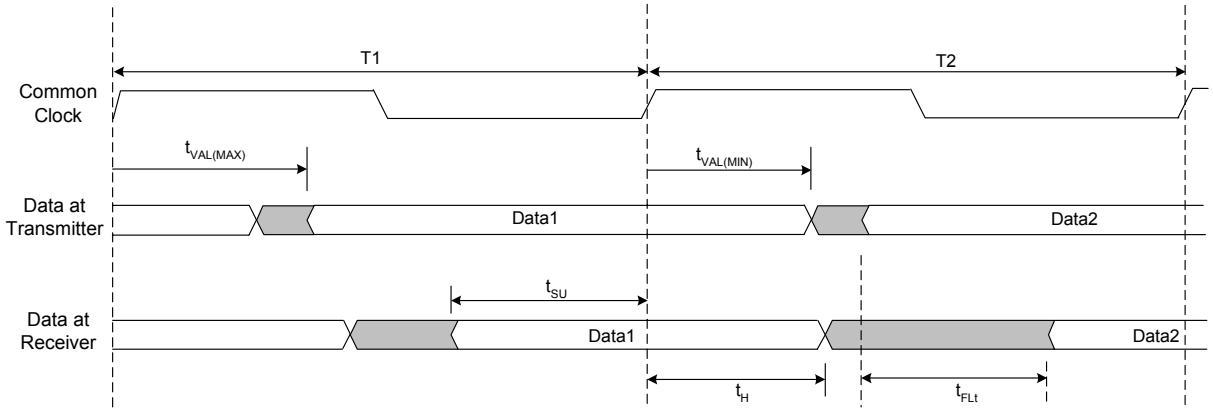


Figure 8-12. AGP 8X Common Clock Transfer Timings

Table 8-6 AGP 8X 66 MHz Common Clock Transfer Timing Parameters

Symbol	Description	Min	Max.	Unit
t_{SKEW}	CLK Skew between AGP 8X devices		1.0	ns
t_{CYC}	CLK cycle time	15	30	ns
t_{HIGH}	CLK high time	6.0		ns

Table 8-6 AGP 8X 66 MHz Common Clock Transfer Timing Parameters (Continued)

Symbol	Description	Min	Max.	Unit
t_{LOW}	CLK low time	6.0		ns
t_{VAL}	CLK to command valid	1.0	5.5	ns
t_{FLT}	Flight time to load		2.5	ns
t_{SU}	Setup to CLK	6.0		ns
t_{H}	Hold from CLK	0		ns
$t_{R,}$ t_{F}	Rise time, Fall time	2.0	3.5	V/ns

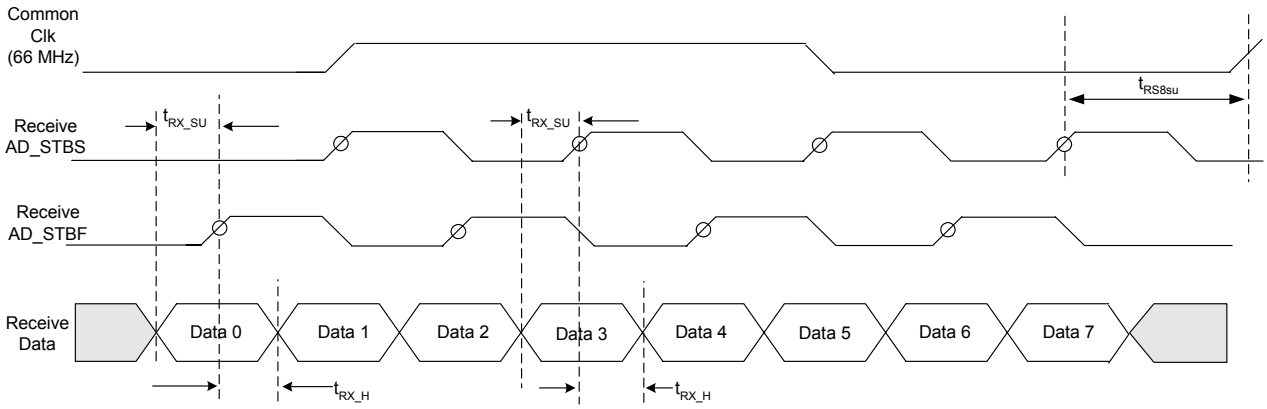


Figure 8-13. Receive Strobe/Data Timings for AGP 8X Source Synchronous Timing

Table 8-7 AGP 8X AC Source-Synchronous Receiver Timing Parameters

Symbol	Description	Min	Max.	Unit
t_{RX_SU}	Receiver setup margin	0	85	ps
t_{RX_H}	Receiver hold margin	0	210	ps
t_{RS8su}	8th AD_STBS rising edge before CLK	6		ns
t_{RS8h}	Receive strobe hold time after CLK	0.5		ns

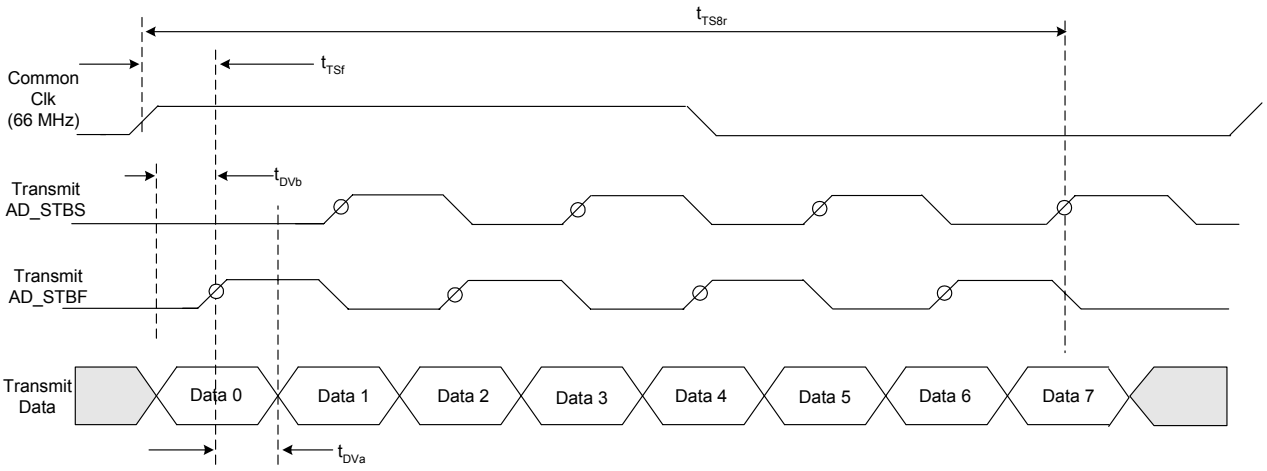


Figure 8-14. Transmit Strobe Timing for AGP 8X Timing

Table 8-8 AGP 8X AC Source-Synchronous Transmitter Timing Parameters

Symbol	Description	Min	Max.	Unit
$t_{BIT\_TIME/2}$	One half bit time	937.5		ps
t_{Dvb}	Data valid before srtobe	527.5		ps
t_{Dva}	Data valid after strobe	477.5		ps
t_{INTC_SUS}	Strobe-to-data skew on setup time caused by interconnect effects	0	442.5	ps
t_{INTC_HS}	Strobe-to-data skew on hold time caused by interconnect effects	0	267.5	ps
t_{TSF}	CLK to first AD_STBF rising edge	1.5		ns
t_{TS8r}	CLK to 4th AD_STBS rising edge		19.5	ns
t_R, t_F	Rise, Fall slew rate	2.0	3.5	V/ns
t_{R-F}	Rise, Fall slew rate matching deviation		25	%

8.2 Memory Timing

8.2.1 Timing Values — Double Data Rate SDRAM/SGRAM

Table 8-9 AC DDR Cycle Timing Values w/o SDRAM DLL

Symbol	Description	Min. (ns)	Max. (ns)
tC	Clock period provided	3.0	15.0 ns
tCH	Clock high time provided	0.5 x tC - 0.15	
tCL	Clock low time provided	0.5 x tC - 0.15	
tCMS	Command setup time provided (RAS, CAS, WE, CS, CKE)	0.5 x tC - 1.0	
tCMH	Command hold time provided (RAS, CAS, WE,CS, CKE)	0.5 x tC + 0.20	
tAS	Address setup time provided	0.5 x tC - 1.0	
tAH	Address hold time provided	0.5 x tC + 0.20	
tWQS	Clock to valid write strobe provided	tC + 0.05	tC + 0.95
tWPRE	Write strobe preamble provided	tC	
tWPST	Write strobe postamble provided	0.5 x tC	
tDQMS	DM setup time provided w.r.t. QS	0.25 x tC - 0.20	
tDQMH	DM hold time provided w.r.t. QS	0.25 x tC - 0.20	
tWDS	Write data setup time provided w.r.t. QS	0.25 x tC - 0.20	
tWDH	Write data hold time provided w.r.t. QS	0.25 x tC - 0.20	
tRQS	Clock to read data strobe required	2.00	0.9 x tC
tRPRE	Read strobe preamble required	tC	
tRPST	Read strobe postamble required	0.5 x tC	
tRDQS	Read data to QS variance required		0.30

Note 1: Write Timing is adjustable in quarter of clock steps.
Note 2: Fine Write Timing adjustments can be done with drivers strength and slew rate settings.
Note 3: Read Timing is adjustable with internal DLL.

Table 8-10 AC Double Data Rate Cycle Timing Values w/ SDRAM DLL

Symbol	Description	Min. (ns)	Max. (ns)
tC	Clock period provided	3.0	15.0 ns
tCH	Clock high time provided	0.5 x tC - 0.15	
tCL	Clock low time provided	0.5 x tC - 0.15	
tCMS	Command setup time provided (RAS, CAS, WE, CS, CKE)	0.5 x tC - 1.0	
tCMH	Command hold time provided (RAS, CAS, WE,CS, CKE)	0.5 x tC + 0.20	
tAS	Address setup time provided	0.5 x tC - 1.0	
tAH	Address hold time provided	0.5 x tC + 0.20	
tWQS	Clock to valid write strobe provided	tC + 0.05	tC + 0.95
tWPRE	Write strobe preamble provided	tC	
tWPST	Write strobe postamble provided	0.5 x tC	
tDQMS	DM setup time provided w.r.t. QS	0.25 x tC - 0.20	
tDQMH	DM hold time provided w.r.t. QS	0.25 x tC - 0.20	
tWDS	Write data setup time provided w.r.t. QS	0.25 x tC - 0.20	
tWDH	Write data hold time provided w.r.t. QS	0.25 x tC - 0.20	
tRQS	Clock to read data strobe required	2.00	0.9 x tC
tRPRE	Read strobe preamble required	tC	
tRPST	Read strobe postamble required	0.5 x tC	

Table 8-10 AC Double Data Rate Cycle Timing Values w/ SDRAM DLL (Continued)

Symbol	Description	Min. (ns)	Max. (ns)
tRDQS	Read data to QS variance required		0.30

Note 1: Write Timing is adjustable in quarter of clock steps.
Note 2: Fine Write Timing adjustments can be done with drivers strength and slew rate settings.
Note 3: Read Timing is adjustable with internal DLL.

8.2.2 Programming Timing Values

Table 8-11 below shows the memory timing parameters that may be programmed through the register MEM_TIMING_CNTL(=0x00000144).

Table 8-11 Programming of Timing Values

Symbol	Description	Min (clocks)	Max (clocks)	Register field in MEM_TIMING_CNTL
tRP	PRE to ACTV minimum delay	2	8	MEM_TRP[10:8]
tRCD	ACTV to CMD Read minimum delay	1	8	MEM_TRCD[2:0]
tRCDW	ACTV to CMD Write minimum delay	1	8	MEM_TRCD[6:4]
tRAS	ACTV to PRE minimum delay	4	19	MEM_TRAS[15:12]
tRRD	ACTV to ACTV minimum delay	1	8	MEM_TRRD[17:16]
tR2W	Read to write data minimum turnaround cycles	CL + 1	CL + 4	MEM_TR2W[19:18]
tWR	Write recovery time	0	7	MEM_TWR[22:20]
tR2R	Different group/rank read to read data minimum turnaround cycles	1	4	MEM_TR2R[29:28]
tW2R	Write to read command delay	0	7	MEM_TW2R[26:24]
tW2RB	Write to read command delay rule	0 - use tW2R	1 - use tWR	MEM_TW2R_SAME_BANK[27]
tRC	Row cycle time	6	27	MEM_TRP[10:8] + MEM_TRAS[15:12]

Table 8-12 below shows the typical values for the above parameters. These values depend on used memory and operating speed.

Table 8-12 Typical Timing Values - DDR

Symbol	Description	Register field in MEM_TIMING_CNTL
tRP	PRE to ACTV minimum delay	MEM_TRP[10:8] = 5 (6 clocks)
tRCD	ACTV to CMD Read minimum delay	MEM_TRCD[2:0] = 3 (4 clocks)
tRCDW	ACTV to CMD Write minimum delay	MEM_TRCDW[6:4] = 4 (5 clocks)
tRAS	ACTV to PRE minimum delay	MEM_TRAS[15:12] = 8 (12 clocks)
tRRD	ACTV to ACTV minimum delay	MEM_TRRD[17:16] = 3 (4 clocks)
tR2W	Read to write data minimum turnaround cycles	MEM_TR2W[19:18] = 3 (CL+4 clocks)
tWR	Write recovery time	MEM_TWR[22:20] = 3 (3 clocks)
tR2R	Different group/rank read to read data minimum turnaround cycles	MEM_TR2R[29:28] = 1 (2 clocks)
tW2R	Write to read command delay	MEM_TW2R_MODE[26:24] = 3 (3 clocks)
tW2RB	Write to read command delay rule	MEM_TW2R_SAME_BANK[29] = 1 (tWR clocks)
tRC	Row cycle time	18 clocks

8.2.3 Double Data Rate (DDR) SGRAM Timing Diagrams

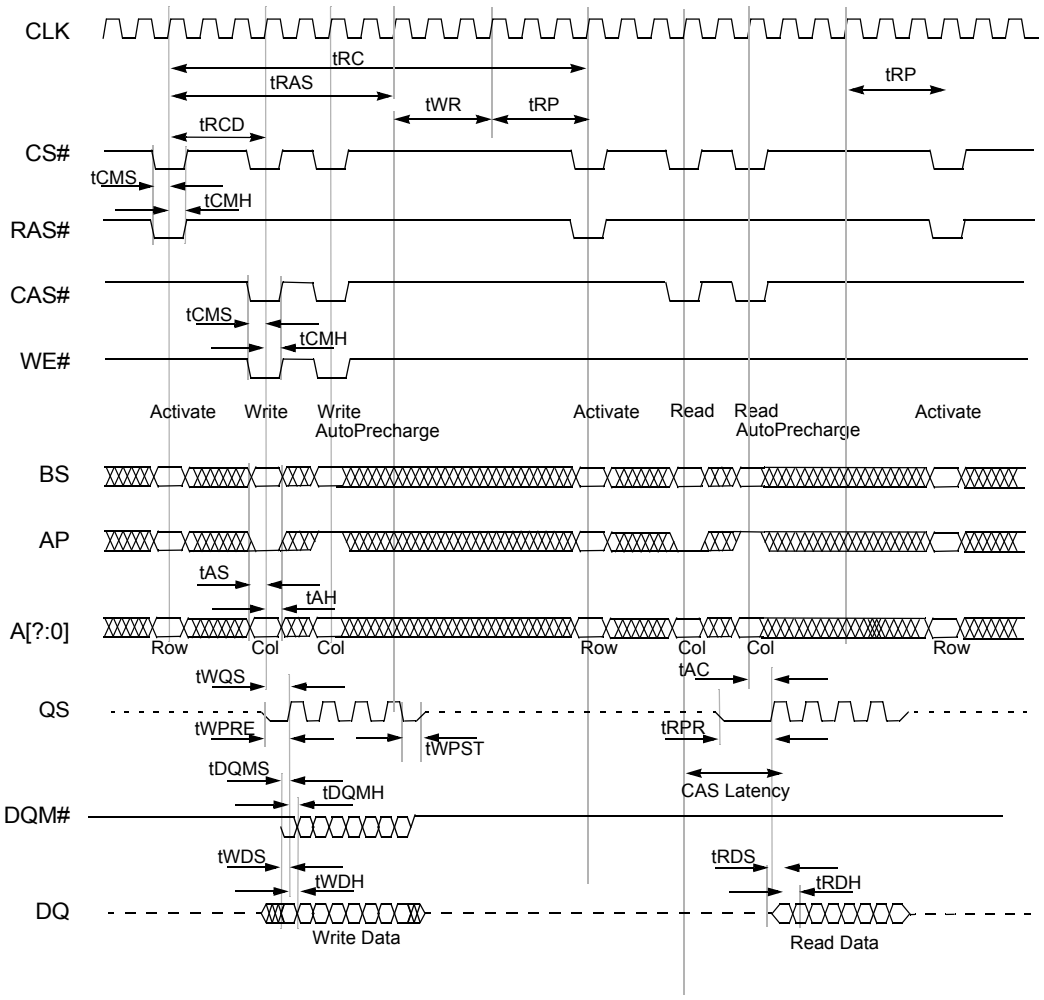


Figure 8-15. SGRAM/SDRAM Basic Read/Write Cycle Timing

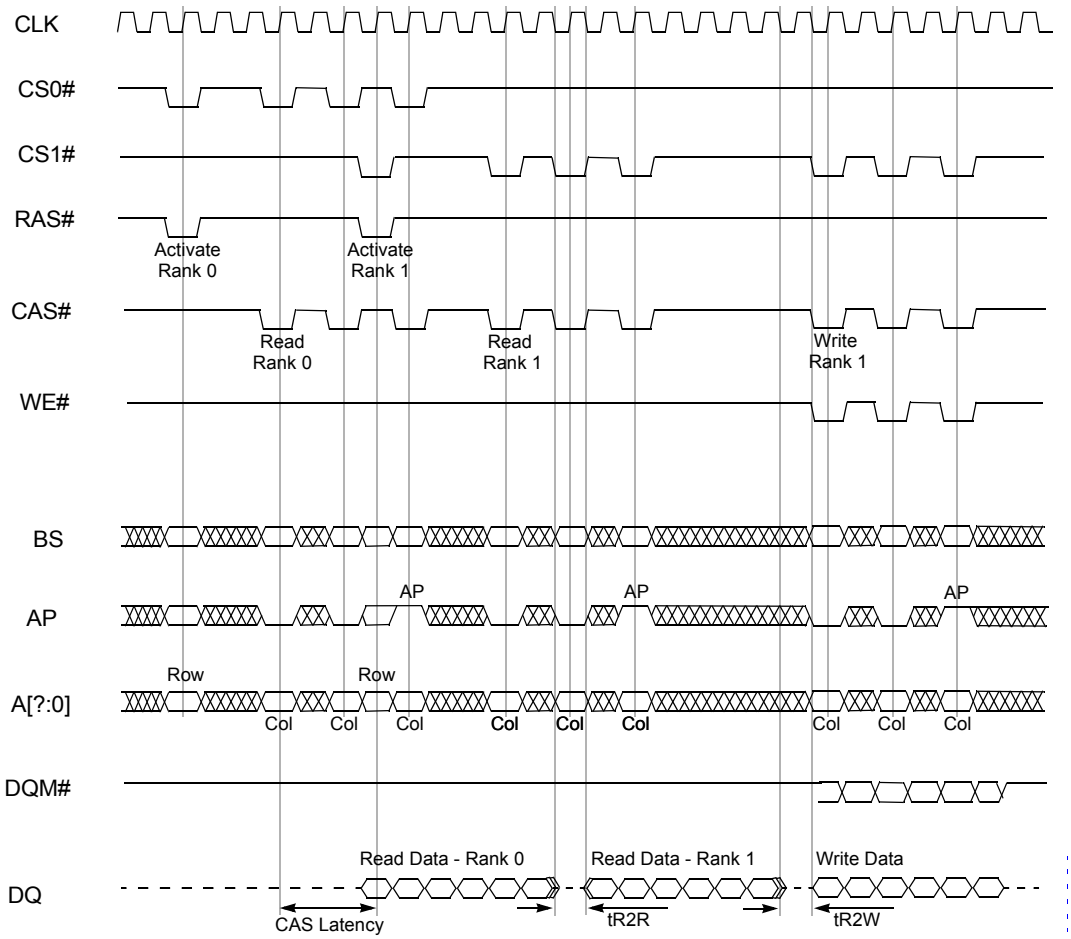


Figure 8-16. Read/Write Data Turnaround Cycles

8.3 I²C Timing

Write Cycle

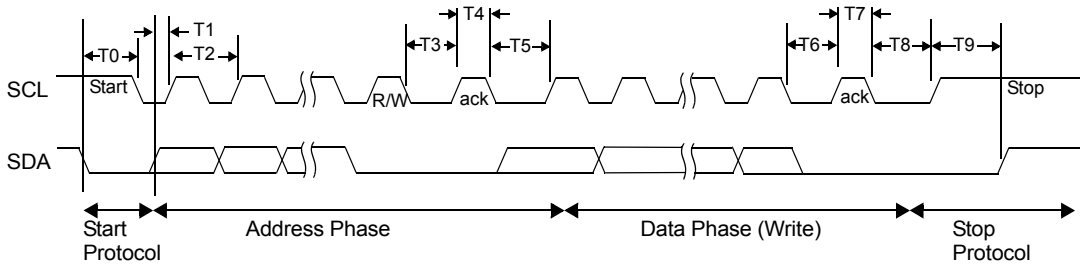


Figure 8-17. I²C Write Cycle

Table 8-13 I²C Write Cycle Timing Parameters

Symbol	Description	Min	Max
T0	Time for the start protocol	$T_{period}/2$	T_{period}
T1	Setup time for outbound address/data	$T_{period}/4$	$T_{period}/4$
T2 (T_{period})	Period of SCL	T_{period}	T_{period}
T3	Time elapse from the R/W bit to ACK	T_{period}	T_{period}
T4	Time for SCL high during ACK	$3T_{period}/4$	$3T_{period}/4$
T5	Time elapse from ACK to the first bit of data	T_{period}	T_{period}
T6	Time elapse from the negative edge of the SCL for the last bit of writing data to the ACK from slave	$7T_{period}/4$	$7T_{period}/4$
T7	Time for SCL high during ACK	$T_{period}/4$	$T_{period}/4$
T8	Time from ACK to STOP protocol	$3T_{period}/4$	$3T_{period}/4$
T9	Setup for stop protocol	$T_{period}/2$	$T_{period}/2$

Read Cycle

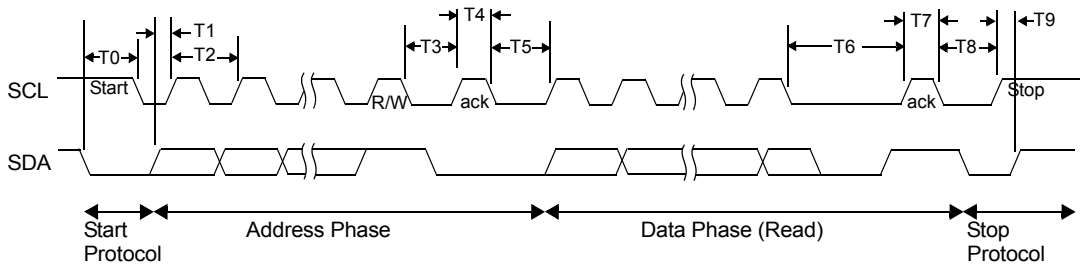


Figure 8-18. I²C Read Cycle

Table 8-14 I²C Read Cycle Timing Parameters

Symbol	Description	Min	Max
T0	Time for the start protocol	$T_{period}/2$	T_{period}
T1	Setup time for outbound address/data	$T_{period}/4$	$T_{period}/4$
T2 (T_{period})	Period of SCL	T_{period}	T_{period}
T3	Time elapse from the R/W bit to ACK	T_{period}	T_{period}
T4	Time for SCL high during ACK	$3T_{period}/4$	$3T_{period}/4$
T5	Time elapse from ACK to the first bit of data	T_{period}	T_{period}
T6	Time elapse from the negative edge of the SCL for the last bit of reading data to ACK from master	$3T_{period}/4$	$3T_{period}/4$
T7	Time for SCL high during ACK	$T_{period}/4$	$T_{period}/4$
T8	Time from ACK to STOP protocol	T_{period}	T_{period}
T9	Setup for stop protocol	$T_{period}/2$	$T_{period}/2$

8.4 VIP Timing

8.4.1 VIP Host Basic Timings and Protocol

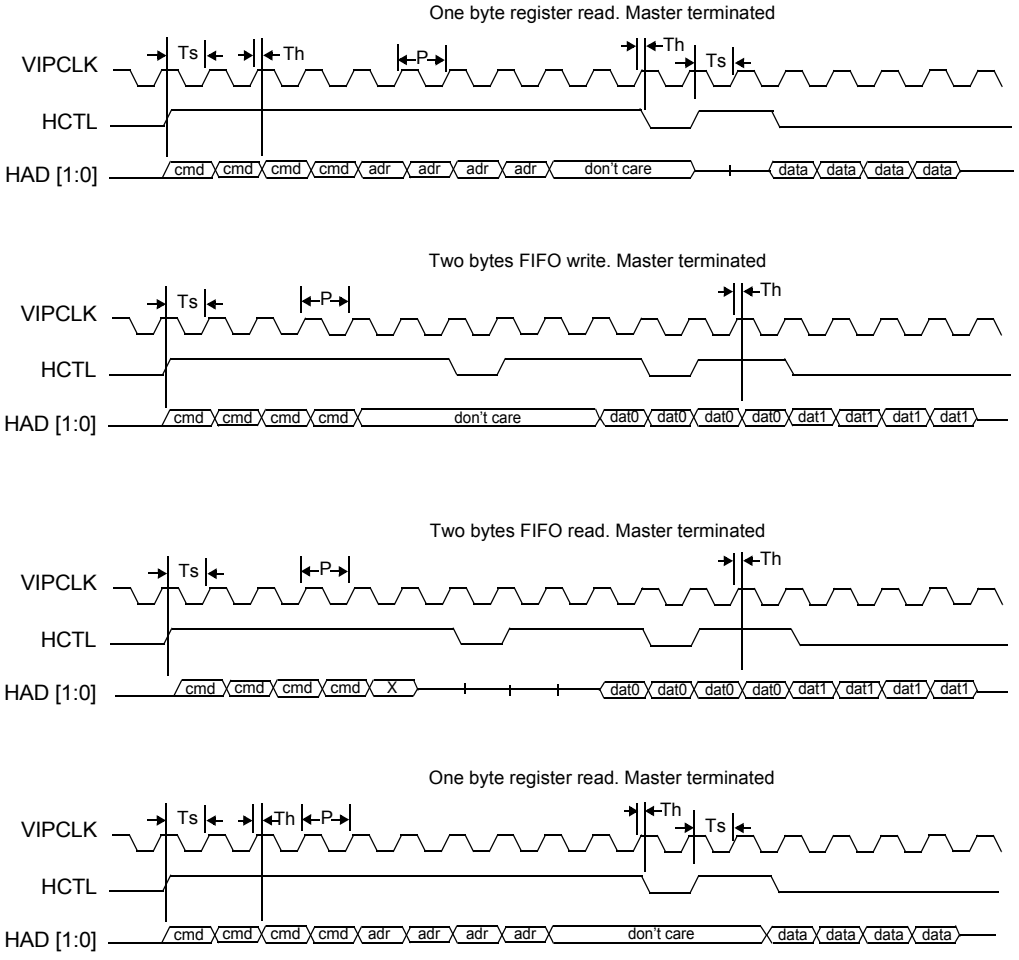


Figure 8-19. VIP Timings and Protocol

Table 8-15 VIP Timing Parameters

Symbol	Description	Min (ns)	Max (ns)
P	Clock period	-	33
Th	Hold time for hctl and had	0	-
Ts	Setup time for hctl and had	5	-

8.5 ROM Read/Write Timing

8.5.1 128K EPROMs, Add-in Board Implementation

The ROM cycle (read/write) is split into two phases:

1- Addresses and ROM control signals are shift-loaded into the external flops in the first phase.

2- The actual ROM cycle (where CE# is asserted).

Note: The timing diagrams for 32K/64K EPROMs are similar except that ROMSI is not used because there is no need for a 17th address bit (A16).

Parallel ROM Write Timing

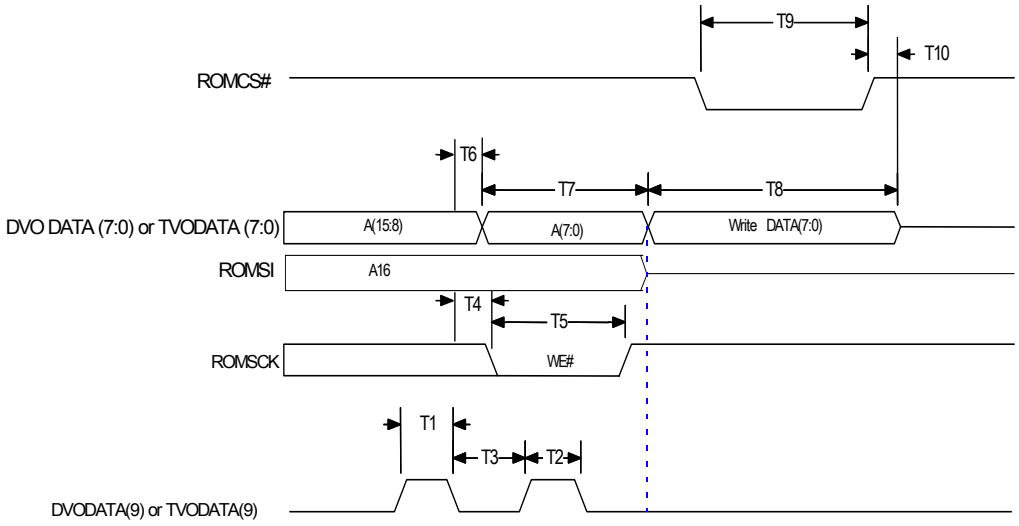


Figure 8-20. Parallel ROM Write Timing

Table 8-16 Parallel ROM Write Timing

Symbol	Description	Time (ns)
T1	First clock high time	2 SCLK
T2	Second clock high time	2 SCLK
T3	Time between the first and the second clock	4 SCLK
T4	Address(16) hold time	2 SCLK
T5	WE# time	(ROM_CLK_DIV + 1) SCLK
T6	Address(15:8) hold time	2 SCLK
T7	Address(7:0) valid time	6 SCLK
T8	Write Data valid	5 + (ROM_CLK_DIV) * 5
T9	CE# asserted time	4 * (ROM_CLK_DIV) SCLK
T10	Write Data hold time	2 SCLK

Note 1: SCLK = Core Clock
Note 2: ROM_CLK_DIV = IN VIDEOMUX_CTL

Parallel ROM Read Timing

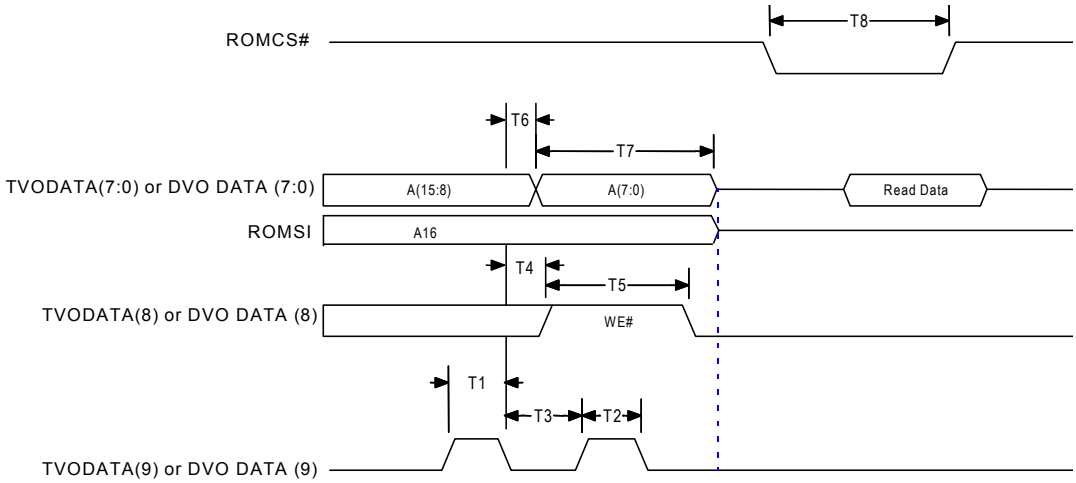


Figure 8-21. Parallel ROM Read Timing

Table 8-17 Parallel ROM Read Timing

Symbol	Description	Time (ns)
T1	First clock high time	2 SCLK
T2	Second clock high time	2 SCLK
T3	Time between the first and the second clock	4 SCLK
T4	Address(16) hold time	2 SCLK
T5	WE# time	(ROM_CLK_DIV + 1) SCLK
T6	Address(15:8) hold time	2 SCLK
T7	Address(7:0) valid time	6 SCLK
T8	CE# asserted time	4 * (ROM_CLK_DIV) SCLK

Note: SCLK = Core Clock

Serial ROM (ST, ATMEL, ISSI) Write/Read Timing

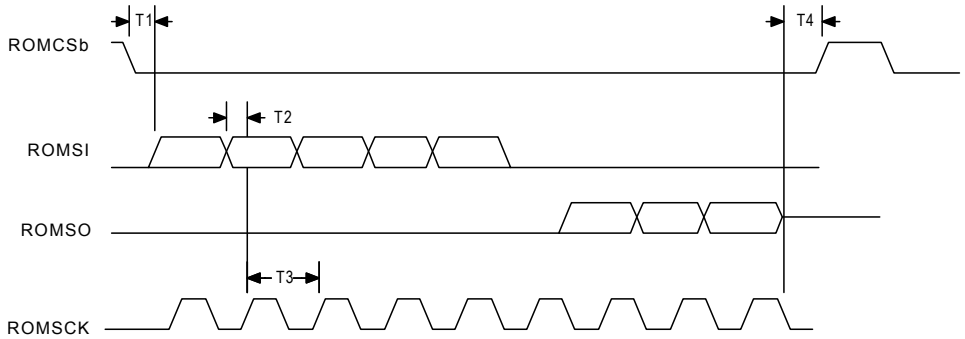


Figure 8-22. Serial ROM (ST, ATMEL, ISSI) Write/Read Timing

Table 8-18 Serial ROM (ST, ATMEL, ISSI) Write/Read Timing

Symbol	Description	Time (ns)
T1	ROMCSb falling edge to valid data sent to the device	5 * (SCK_PRESCALE + 1) + 1 SCLK
T2	Input data to the device setup time	¼ * (SCK_PRESCALE + 1) + 3 SCLK
T3	Serial Clock period	(SCK_PRESCALE + 1) * 2
T4	Last clock cycle to ROMCSb rising edge	16 * (SCK_PRESCALE + 1) * WAIT_CYCLE - 1

Note: SCK_PRESCALE = Register in RADEON 9800

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Chapter 9
EXOR Tree

9.1 Brief Description of an EXOR Tree

A sample of a generic EXOR tree is shown in the figure below.

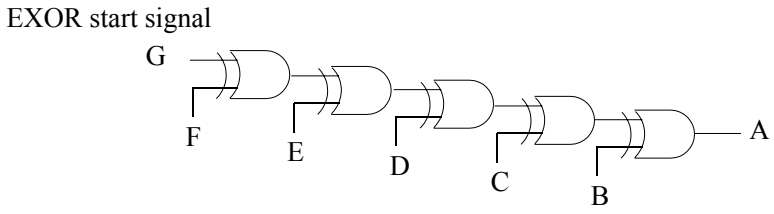

Figure 9-1. Sample of an EXOR Tree

Pin A is assigned to the output direction, and pins B through F are assigned to the input direction. It can be seen that after all pins B to F are assigned a logic '0' or '1', a logic change in any one of these pins will toggle the output pin A. The truth table is shown below.

Table 9-1 EXOR Tree Truth Table

G	F	E	D	C	B	A
0	0	0	0	0	0	0
1	0	0	0	0	0	1
1	1	0	0	0	0	0
1	1	1	0	0	0	1
1	1	1	1	0	0	0
1	1	1	1	1	0	1
1	1	1	1	1	1	0

9.2 Description of the RADEON 9800 EXOR Tree

9.2.1 JTAG Mapping

The following RADEON 9800 pins are mapped to the JTAG functional pins:

Table 9-2 RADEON 9000 Series-JTAG Pin Mapping

JTAG	RADEON 9800
TMS (Test Mode Select)	VID(7)
TDI (Test Data Input)	VID(5)
TCLK (Test Clock)	VID(6)
TDO (Test Data Output)	VID(4)
TRST (Test Reset)	VID(3)

9.2.2 JTAG Instruction for EXOR Tree

The TESTEN pin is used to assert test mode. When TESTEN is set to logic '1' and TCLK is connected to a clock, the values of TDI and TMS will be set to proper values. When the tap controller of JTAG is set to Shift-IR mode, the EXOR-tree mode should be shifted in by TDI: 00001000.

For input pins in the EXOR tree that are not connected to package balls, the internal pull-up and pull-down resistors can be activated by JTAG instructions, 00110000 for pull-up, and 00110011 for pull-down.

High Impedance Mode (HIGH_Z)

In this mode, all bi-directional pins are forced to the input direction, and all pure output pins (such as XTALOUT) are forced to high impedance. Note that only the directions of digital pins are controlled by this test mode. Analog pins and power/ground pins are not affected. JTAG instruction for HIGH_Z is: 00000011.

9.2.3 Testing Procedure

1 Enable TESTEN.
2 The external pins SCAN_MODE, SCAN_ENABLE should all be pulled low.
3 Pull up external AGP8X_DETB strap pin. (Might not be necessary)
4 Bring the chip out of reset.
5 Use the JTAG interface to set the “tc_cg_test_sel” field of the CLKCTRL tap register to 3. This puts the chip clocking in scan clock mode so that TEST_YCLK will be used as YCLK.
6 Drive TEST_YCLK with some clock so that the outputs eventually appear on the output pins flopped by YCLK.
7 Use the JTAG interface to set only the following bits in the IOCTRL tap register:
   a. intercept = 1 (enables test pad controls)
   b. pad_pu = 1 (disable pullups on pads)
   c. pad_mode = 1 (puts pads in test mode)
   d. pad_tsto = 2 (turns on alternating i/o test)
   e. pad_schmen = 1 (enables input on test inputs)
   f. tste_odd = 0/1 (1 if the odd pads are the output pads)
   g. tste_even= 0/1 (1 if the even pads are the output pads)
   h. pad_imp = 1 (disable impedance control)
8 Apply inputs to the input pads and look at the output on JTAG TDO.

9.2.4 RADEON 9800 EXOR Tree Connection Order

The table next page shows the order of the EXOR tree connections.

Note: All the power and ground pins, analog pins are not part of the EXOR tree.

Table 9-3 RADEON 9800 Exor Tree Order

#	Pin Name	#	Pin Name	#	Pin Name	#	Pin Name
1	DQA[39]	46	DQA[14]	91	AD[13]	136	AGP8X_DETB
2	DQA[38]	47	DQA[13]	92	AD[14]	137	RSTB
3	DQA[37]	48	DQA[12]	93	AD[15]	138	PCICLK
4	DQA[36]	49	QSA[1]	94	C_BEB[1]	139	TEST_AGPCLK
5	QSA[4]	50	DQMAB[1]	95	TRDYB	140	PSYNC
6	DQMAB[4]	51	DQA[11]	96	STOPB	141	DVALID
7	DQA[35]	52	DQA[10]	97	DEVSELB	142	VPCLK0
8	DQA[34]	53	DQA[9]	98	FRAMEB	143	VID[1]
9	DQA[33]	54	DQA[8]	99	IRDYB	144	DDC2CLK
10	DQA[32]	55	RDCMDA	100	PAR	145	DDC2DATA
11	DIMA[1]	56	DQA[23]	101	AD[16]	146	HPD1
12	WEAB	57	DQA[22]	102	C_BEB[2]	147	V2SYNC
13	CASAB	58	DQA[21]	103	AD[18]	148	H2SYNC
14	RASAB	59	DQA[20]	104	AD[17]	149	HPD2
15	CSAB	60	QSA[2]	105	AD[20]	150	DDC1DATA
16	CKEA	61	DQMAB[2]	106	AD[19]	151	DDC1CLK
17	MAA[13]	62	DQA[19]	107	AD[22]	152	STEREOSYNC
18	MAA[14]	63	DQA[18]	108	AD[21]	153	HSYNC
19	MAA[7]	64	DQA[17]	109	C_BEB[3]	154	VSYNC
20	MAA[12]	65	DQA[16]	110	AD[23]	155	AUXWIN
21	MAA[8]	66	DQA[31]	111	AD_STBF[1]	156	ROMCSB
22	CLKA1	67	DQA[30]	112	AD[24]	157	ROMSCK
23	CLKA0	68	DQA[29]	113	AD[25]	158	ROMSO
24	MAA[1]	69	DQA[28]	114	AD[26]	159	ROMSI
25	MAA[6]	70	QSA[3]	115	AD[27]	160	SDA
26	MAA[0]	71	DQMAB[3]	116	AD[28]	161	SCL
27	MAA[2]	72	DQA[27]	117	AD[29]	162	VHAD[1]
28	MAA[5]	73	DQA[26]	118	AD[30]	163	VHAD[0]
29	MAA[3]	74	DQA[25]	119	AD[31]	164	VPHCTL
30	MAA[4]	75	DQA[24]	120	SBA[7]	165	VIPCLK
31	MAA[11]	76	AD[0]	121	SBA[6]	166	TVOCLKO
32	MAA[10]	77	AD[1]	122	SBA[5]	167	TVOCLKI
33	MAA[9]	78	AD[2]	123	SBA[4]	168	TVODATA[9]
34	DQA[7]	79	AD[3]	124	SB_STBF	169	TVODATA[8]
35	DQA[6]	80	AD[4]	125	SBA[3]	170	TVODATA[7]
36	DQA[5]	81	AD[5]	126	SBA[2]	171	TVODATA[6]
37	DQA[4]	82	AD[6]	127	SBA[1]	172	TVODATA[5]
38	QSA[0]	83	AD[7]	128	SBA[0]	173	TVODATA[4]
39	DQMAB[0]	84	AD_STBF[0]	129	ST[1]	174	TVODATA[3]
40	DQA[3]	85	C_BEB[0]	130	ST[0]	175	TVODATA[2]
41	DQA[2]	86	AD[8]	131	ST[2]	176	TVODATA[1]
42	DQA[1]	87	AD[9]	132	RBFB	177	TVODATA[0]
43	DQA[0]	88	AD[10]	133	WBFB	178	DVODATA[11]
44	DIMA[0]	89	AD[11]	134	REQB	179	DVODATA[10]
45	DQA[15]	90	AD[12]	135	GNTB	180	DVODATA[9]

Table 9-3 RADEON 9800 Exor Tree Order

#	Pin Name	#	Pin Name	#	Pin Name	#	Pin Name
181	DVODATA[8]	227	DQD[36]	273	DQMDB[1]	319	DQC[46]
182	DVODATA[7]	228	QSD[4]	274	DQD[11]	320	DQC[45]
183	DVODATA[6]	229	DQMDB[4]	275	DQD[10]	321	DQC[44]
184	DVODATA[5]	230	DQD[35]	276	DQD[9]	322	QSC[5]
185	DVODATA[4]	231	DQD[34]	277	DQD[8]	323	DQMCB[5]
186	DVODATA[3]	232	DQD[33]	278	DQD[23]	324	DQC[43]
187	DVODATA[2]	233	DQD[32]	279	DQD[22]	325	DQC[42]
188	DVODATA[1]	234	DIMD[1]	280	DQD[21]	326	DQC[41]
189	DVODATA[0]	235	WEDB	281	DQD[20]	327	DQC[40]
190	DVOCNTL[0]	236	CASDB	282	QSD[2]	328	RDCMDC
191	DVOCNTL[1]	237	RASDB	283	DQMDB[2]	329	DQC[39]
192	DVOCNTL[2]	238	CSDB	284	DQD[19]	330	DQC[38]
193	DQD[63]	239	CKED	285	DQD[18]	331	DQC[37]
194	DQD[62]	240	MAD[13]	286	DQD[17]	332	DQC[36]
195	DQD[61]	241	MAD[14]	287	DQD[16]	333	QSC[4]
196	DQD[60]	242	MAD[7]	288	DQD[31]	334	DQMCB[4]
197	QSD[7]	243	MAD[12]	289	DQD[30]	335	DQC[35]
198	DQMDB[7]	244	MAD[8]	290	DQD[29]	336	DQC[34]
199	DQD[59]	245	CLKD1	291	DQD[28]	337	DQC[33]
200	DQD[58]	246	CLKD0	292	QSD[3]	338	DQC[32]
201	DQD[57]	247	MAD[1]	293	DQMDB[3]	339	DIMC[1]
202	DQD[56]	248	MAD[6]	294	DQD[27]	340	WECB
203	DQD[55]	249	MAD[0]	295	DQD[26]	341	CASCB
204	DQD[54]	250	MAD[2]	296	DQD[25]	342	RASCB
205	DQD[53]	251	MAD[5]	297	DQD[24]	343	CSCB
206	DQD[52]	252	MAD[3]	298	DQC[63]	344	CKEC
207	QSD[6]	253	MAD[4]	299	DQC[62]	345	MAC[13]
208	DQMDB[6]	254	MAD[11]	300	DQC[61]	346	MAC[14]
209	DQD[51]	255	MAD[10]	301	DQC[60]	347	MAC[7]
210	DQD[50]	256	MAD[9]	302	QSC[7]	348	MAC[12]
211	DQD[49]	257	DQD[7]	303	DQMCB[7]	349	MAC[8]
212	DQD[48]	258	DQD[6]	304	DQC[59]	350	CLKC1
213	DQD[47]	259	DQD[5]	305	DQC[58]	351	CLKC0
214	DQD[46]	260	DQD[4]	306	DQC[57]	352	MAC[1]
215	DQD[45]	261	QSD[0]	307	DQC[56]	353	MAC[6]
216	DQD[44]	262	DQMDB[0]	308	DQC[55]	354	MAC[0]
217	QSD[5]	263	DQD[3]	309	DQC[54]	355	MAC[2]
218	DQMDB[5]	264	DQD[2]	310	DQC[53]	356	MAC[5]
219	DQD[43]	265	DQD[1]	311	DQC[52]	357	MAC[3]
220	DQD[42]	266	DQD[0]	312	QSC[6]	358	MAC[4]
221	DQD[41]	267	DIMD[0]	313	DQMCB[6]	359	MAC[11]
222	DQD[40]	268	DQD[15]	314	DQC[51]	360	MAC[10]
223	RDCMDD	269	DQD[14]	315	DQC[50]	361	MAC[9]
224	DQD[39]	270	DQD[13]	316	DQC[49]	362	DQC[7]
225	DQD[38]	271	DQD[12]	317	DQC[48]	363	DQC[6]
226	DQD[37]	272	QSD[1]	318	DQC[47]	364	DQC[5]

Table 9-3 RADEON 9800 Exor Tree Order

#	Pin Name	#	Pin Name	#	Pin Name	#	Pin Name
365	DQC[4]	411	DQB[57]	457	MAB[6]	503	DQMBB[3]
366	QSC[0]	412	DQB[56]	458	MAB[0]	504	DQB[27]
367	DQMCB[0]	413	DQB[55]	459	MAB[2]	505	DQB[26]
368	DQC[3]	414	DQB[54]	460	MAB[5]	506	DQB[25]
369	DQC[2]	415	DQB[53]	461	MAB[3]	507	DQB[24]
370	DQC[1]	416	DQB[52]	462	MAB[4]	508	DQA[63]
371	DQC[0]	417	QSB[6]	463	MAB[11]	509	DQA[62]
372	DIMC[0]	418	DQMBB[6]	464	MAB[10]	510	DQA[61]
373	DQC[15]	419	DQB[51]	465	MAB[9]	511	DQA[60]
374	DQC[14]	420	DQB[50]	466	DQB[7]	512	QSA[7]
375	DQC[13]	421	DQB[49]	467	DQB[6]	513	DQMAB[7]
376	DQC[12]	422	DQB[48]	468	DQB[5]	514	DQA[59]
377	QSC[1]	423	DQB[47]	469	DQB[4]	515	DQA[58]
378	DQMCB[1]	424	DQB[46]	470	QSB[0]	516	DQA[57]
379	DQC[11]	425	DQB[45]	471	DQMBB[0]	517	DQA[56]
380	DQC[10]	426	DQB[44]	472	DQB[3]	518	DQA[55]
381	DQC[9]	427	QSB[5]	473	DQB[2]	519	DQA[54]
382	DQC[8]	428	DQMBB[5]	474	DQB[1]	520	DQA[53]
383	DQC[23]	429	DQB[43]	475	DQB[0]	521	DQA[52]
384	DQC[22]	430	DQB[42]	476	DIMB[0]	522	QSA[6]
385	DQC[21]	431	DQB[41]	477	DQB[15]	523	DQMAB[6]
386	DQC[20]	432	DQB[40]	478	DQB[14]	524	DQA[51]
387	QSC[2]	433	DQB[39]	479	DQB[13]	525	DQA[50]
388	DQMCB[2]	434	DQB[38]	480	DQB[12]	526	DQA[49]
389	DQC[19]	435	DQB[37]	481	QSB[1]	527	DQA[48]
390	DQC[18]	436	DQB[36]	482	DQMBB[1]	528	DQA[47]
391	DQC[17]	437	QSB[4]	483	DQB[11]	529	DQA[46]
392	DQC[16]	438	DQMBB[4]	484	DQB[10]	530	DQA[45]
393	DQC[31]	439	DQB[35]	485	DQB[9]	531	DQA[44]
394	DQC[30]	440	DQB[34]	486	DQB[8]	532	QSA[5]
395	DQC[29]	441	DQB[33]	487	RDCMDB	533	DQMAB[5]
396	DQC[28]	442	DQB[32]	488	DQB[23]	534	DQA[43]
397	QSC[3]	443	DIMB[1]	489	DQB[22]	535	DQA[42]
398	DQMCB[3]	444	WEBB	490	DQB[21]	536	DQA[41]
399	DQC[27]	445	CASBB	491	DQB[20]	537	DQA[40]
400	DQC[26]	446	RASBB	492	QSB[2]		
401	DQC[25]	447	CSBB	493	DQMBB[2]		
402	DQC[24]	448	CKEB	494	DQB[19]		
403	DQB[63]	449	MAB[13]	495	DQB[18]		
404	DQB[62]	450	MAB[14]	496	DQB[17]		
405	DQB[61]	451	MAB[7]	497	DQB[16]		
406	DQB[60]	452	MAB[12]	498	DQB[31]		
407	QSB[7]	453	MAB[8]	499	DQB[30]		
408	DQMBB[7]	454	CLKB1	500	DQB[29]		
409	DQB[59]	455	CLKB0	501	DQB[28]		
410	DQB[58]	456	MAB[1]	502	QSB[3]		

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Appendix A
Pin Listings

This appendix contains pin listings for the RADEON 9800 sorted in different ways. To go to the listing of interest, use the following list of linked cross references:

"RADEON 9800 Pin List Sorted by Ball Reference" on page A-2

"RADEON 9800 Pin List Sorted by Signal Name" on page A-15

A.1 RADEON 9800 Pin List Sorted by Ball Reference

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference

Ball Ref	Signal
A10	DQB49
A11	DQB39
A12	DQB37
A13	QSB4
A14	DQB35
A15	DQB33
A16	CASB#
A17	CKEB
A18	MAB12
A19	CLKB1#
A2	DQC28
A20	CLKB0
A21	DIMB0
A22	DQB15
A23	DQB13
A24	QSB1
A25	DQB11
A26	DQB9
A27	DQB31
A28	DQB29
A29	QSB3
A3	QSC3
A30	DQB27
A31	DQB25
A32	DQA55
A33	DQA53
A34	QSA6
A35	DQA51
A36	DQA49
A37	DQA39
A38	DQA37
A4	DQC27
A5	DQC25
A6	DQB55
A7	DQB53
A8	QSB6
A9	DQB51
AA1	QSC6
AA13	VSS
AA14	VSS
AA15	VSS
AA16	VSS

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
AA17	VSS
AA18	VSS
AA19	VSS
AA2	DQMC#6
AA20	VSS
AA21	VSS
AA22	VSS
AA23	VSS
AA24	VSS
AA25	VSS
AA26	VSS
AA27	VSS
AA3	DQC57
AA33	VDDP
AA34	VSSP
AA35	PAR
AA36	AD2
AA37	AD3
AA38	AD18
AA39	CBE#2
AA4	DQC56
AA5	DQC47
AA6	VDDR1
AA7	VDDR1
AB1	DQC53
AB13	VSS
AB14	VSS
AB15	VSS
AB16	VSS
AB17	VSS
AB18	VSS
AB19	VSS
AB2	DQC52
AB20	VSS
AB21	VSS
AB22	VSS
AB23	VSS
AB24	VSS
AB25	VSS
AB26	VSS
AB27	VSS
AB3	DQMC#7
AB33	VDDP
AB34	VDDP
AB35	STOP#

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
AB36	AD4
AB37	AD5
AB38	AD20
AB39	AD17
AB4	DQC59
AB5	DQC58
AB6	VDDR1
AB7	VDDR1
AC1	DQC55
AC13	VDDCI
AC14	VDDC
AC15	VDDC
AC16	VDDC
AC17	VDDC
AC18	VSS
AC19	VSS
AC2	DQC54
AC20	VSS
AC21	VSS
AC22	VSS
AC23	VDDC
AC24	VDDC
AC25	VDDC
AC26	VDDC
AC27	VDDCI
AC3	DQC60
AC33	VDDP
AC34	VSSP
AC35	VSSP
AC36	AD6
AC37	VSSP
AC38	AD22
AC39	AD19
AC4	QSC7
AC5	VSS
AC6	VREF1
AC7	VSS
AD1	DQD25
AD13	VDDC
AD14	VDDC
AD15	VDDC
AD16	VDDC
AD17	VDDC
AD18	VSS
AD19	VSS

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
AD2	DQD24
AD20	VSS
AD21	VSS
AD22	VSS
AD23	VDDC
AD24	VDDC
AD25	VDDC
AD26	VDDC
AD27	VDDC
AD3	VSS
AD33	VDDP
AD34	VSSP
AD35	DEVSEL#
AD36	AD_STBS0
AD37	AD7
AD38	CBE#3
AD39	AD21
AD4	DQC62
AD5	DQC61
AD6	VDDR1
AD7	VSS
AE1	DQD27
AE13	VDDC
AE14	VDDC
AE15	VDDC
AE16	VDDC
AE17	VDDC
AE18	VSS
AE19	VSS
AE2	DQD26
AE20	VSS
AE21	VSS
AE22	VSS
AE23	VDDC
AE24	VDDC
AE25	VDDC
AE26	VDDC
AE27	VDDC
AE3	DQD17
AE33	VDDP
AE34	VSSP
AE35	TRDY#
AE36	VSSP
AE37	AD_STBF0
AE38	AD_STBS1

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
AE39	AD23
AE4	DQD16
AE5	DQC63
AE6	VDDR1
AE7	VSS
AF1	QSD3
AF13	VDDC
AF14	VDDC
AF15	VDDC
AF16	VDDC
AF17	VDDC
AF18	VSS
AF19	VSS
AF2	DQMD#3
AF20	VSS
AF21	VSS
AF22	VSS
AF23	VDDC
AF24	VDDC
AF25	VDDC
AF26	VDDC
AF27	VDDC
AF3	DQMD#2
AF33	VDDP
AF34	VDDP
AF35	VSSP
AF36	CBE#0
AF37	AD8
AF38	VSSP
AF39	AD_STBF1
AF4	DQD19
AF5	DQD18
AF6	VSS
AF7	VDDR1
AG1	DQD29
AG13	VDDC
AG14	VDDC
AG15	VDDC
AG16	VDDC
AG17	VDDC
AG18	VSS
AG19	VSS
AG2	DQD28
AG20	VSS
AG21	VSS

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
AG22	VSS
AG23	VDDCI
AG24	VDDC
AG25	VDDC
AG26	VDDC
AG27	VDDC
AG3	DQD20
AG33	VDDP
AG34	AGPREF
AG35	FRAME#
AG36	AD9
AG37	AD10
AG38	AD25
AG39	AD24
AG4	QSD2
AG5	VT1
AG6	VSS
AG7	VDDR1
AH1	DQD31
AH2	DQD30
AH3	VSS
AH33	VDDP
AH34	VSSP
AH35	IRDY#
AH36	AD11
AH37	AD12
AH38	AD27
AH39	AD26
AH4	DQD22
AH5	DQD21
AH6	VT2
AH7	VSS
AJ1	DQD9
AJ2	DQD8
AJ3	DQD1
AJ33	VDDP
AJ34	VDDP
AJ35	VSSP
AJ36	AD13
AJ37	VSSP
AJ38	AD29
AJ39	AD28
AJ4	DQD0
AJ5	DQD23
AJ6	VDDR1

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
AJ7	VSS
AK1	DQD11
AK2	DQD10
AK3	DQMD#0
AK33	VDDP
AK34	VSSP
AK35	VSSP
AK36	AD15
AK37	AD14
AK38	AD31
AK39	AD30
AK4	DQD3
AK5	DQD2
AK6	VSS
AK7	VDDC18
AL1	QSD1
AL2	DQMD#1
AL3	DQD4
AL33	VDDP
AL34	VSSP
AL35	AGP8X_DET#
AL36	AGPTEST
AL37	CBE#1
AL38	DBI_HI
AL39	DBI_LO
AL4	QSD0
AL5	VSS
AL6	VDDR1
AL7	VDDRH
AM1	DQD13
AM2	DQD12
AM3	VSS
AM33	VSSP
AM34	VDDP
AM35	VSSP
AM36	WBF#
AM37	VSSP
AM38	VSSP
AM39	RBF#
AM4	DQD6
AM5	DQD5
AM6	VDDR1
AM7	VSSRH
AN1	DQD15
AN10	VSS

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
AN11	VSS
AN12	VDDR1
AN13	VDDR1
AN14	VDDR1
AN15	VSS
AN16	VSS
AN17	VDDR4
AN18	VDDR4
AN19	VSS
AN2	DQD14
AN20	VSS
AN21	VDDR2
AN22	VDDC18
AN23	VSS
AN24	VSS
AN25	VDDR3
AN26	VSS
AN27	VDDC18
AN28	VDDR3
AN29	VDDR3
AN3	MAD10
AN30	VSS
AN31	VSS
AN32	VDDC18
AN33	VDDP
AN34	VDDP
AN35	VSSP
AN36	SBA6
AN37	SBA7
AN38	ST2
AN39	ST1
AN4	MAD11
AN5	DQD7
AN6	VDDR1
AN7	VDDC
AN8	VDDR1
AN9	VDDR1
AP1	DIMD0
AP10	VDDR1
AP11	VDDR1
AP12	VDDR1
AP13	VSS
AP14	VSS
AP15	VDDR4
AP16	VDDR4

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
AP17	VSS
AP18	VSS
AP19	VDDR2
AP2	CLKD0#
AP20	VDDR2
AP21	VSS
AP22	VSS
AP23	VSS
AP24	VDDR3
AP25	VSS
AP26	VDDR3
AP27	VDDR3
AP28	VSS
AP29	ROMSO
AP3	MAD3
AP30	ROMSCK
AP31	AUXWIN
AP32	STEREOSYNC
AP33	TEST_AGPCLK
AP34	VSS
AP35	RST#
AP36	SBA4
AP37	SBA5
AP38	GNT#
AP39	ST0
AP4	MAD9
AP5	VSS
AP6	VDDC
AP7	VDDR1
AP8	VDDR1
AP9	VSS
AR1	CLKD0
AR10	DQD45
AR11	DQD56
AR12	VSS
AR13	QSD7
AR14	DQD61
AR15	DVODATA1
AR16	VDDR4
AR17	DVODATA8
AR18	VSS
AR19	TVOVMODE
AR2	VSS
AR20	VSS
AR21	VSS

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
AR22	VDDR3
AR23	VDDR3
AR24	AVSSN1
AR25	VDDR3
AR26	VSS
AR27	SCL
AR28	SDA
AR29	ROMSI
AR3	MAD5
AR30	ROMCS#
AR31	HPD1
AR32	H2SYNC
AR33	HPD2
AR34	DDC2CLK
AR35	DDC2DATA
AR36	VSSP
AR37	SB_STBS
AR38	SB_STBF
AR39	SBA3
AR4	MAD2
AR5	VDDC
AR6	MAD4
AR7	DIMD1
AR8	DQD42
AR9	QSD5
AT1	CLKD1#
AT10	DQD46
AT11	DQD57
AT12	DQD59
AT13	DQD60
AT14	DQD62
AT15	DVODATA0
AT16	DVODATA5
AT17	DVODATA7
AT18	DVOVMODE
AT19	TVODATA3
AT2	CLKD1
AT20	TVODATA7
AT21	TVODATA9
AT22	VSS
AT23	VSS
AT24	AVSSN2
AT25	A2VSSN1
AT26	VSS2DI
AT27	A2VSSQ

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
AT28	TXVDDR2
AT29	TXVDDR1
AT3	MAD0
AT30	VSYNC
AT31	HSYNC
AT32	V2SYNC
AT33	VHAD1
AT34	VID7
AT35	VID3
AT36	TESTEN
AT37	SBA0
AT38	SBA1
AT39	SBA2
AT4	VDDC
AT5	MAD6
AT6	MAD1
AT7	DQD40
AT8	DQD43
AT9	DQD44
AU1	MAD13
AU10	DQD47
AU11	DQD58
AU12	DQMD#7
AU13	VSS
AU14	DQD63
AU15	DVOCNTL0
AU16	DVODATA4
AU17	DVODATA6
AU18	DVODATA11
AU19	TVODATA2
AU2	MAD8
AU20	TVODATA6
AU21	TVODATA8
AU22	AVSSQ
AU23	VDD1DI
AU24	VSS1DI
AU25	A2VDDQ
AU26	A2VSSN2
AU27	VDD2DI
AU28	TXVSSR1
AU29	TXVSSR2
AU3	VDDC
AU30	TXVSSR3
AU31	DDC1CLK
AU32	DDC1DATA

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
AU33	VHAD0
AU34	VID6
AU35	VID2
AU36	DVALID
AU37	INTA#
AU38	VSSP
AU39	REQ#
AU4	MAD12
AU5	MAD7
AU6	VSS
AU7	DQD41
AU8	DQMD#5
AU9	VSS
AV1	CKED
AV10	DQD48
AV11	DQD50
AV12	DQMD#6
AV13	DQD52
AV14	DQD54
AV15	DVOCNTL1
AV16	DVODATA3
AV17	DVOCLK1
AV18	DVODATA10
AV19	TVODATA1
AV2	VDDC
AV20	TVODATA5
AV21	TVOCLKI
AV22	RSET
AV23	AVDD1
AV24	AVDD2
AV25	R2SET
AV26	A2VDD1
AV27	A2VDD2
AV28	TPVSS
AV29	TXCM
AV3	CSD#
AV30	TX0M
AV31	TX1M
AV32	TX2M
AV33	VIPCLK
AV34	VID5
AV35	VID1
AV36	PSYNC
AV37	PVSS
AV38	XTALIN

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
AV39	PCICLK
AV4	MAD14
AV5	DQD32
AV6	DQD34
AV7	DQMD#4
AV8	DQD36
AV9	DQD38
AW10	DQD49
AW11	DQD51
AW12	QSD6
AW13	DQD53
AW14	DQD55
AW15	DVOCNTL2
AW16	DVODATA2
AW17	DVOCLK0
AW18	DVODATA9
AW19	TVODATA0
AW2	CASD#
AW20	TVODATA4
AW21	TVOCLKO
AW22	B
AW23	G
AW24	R
AW25	COMP_B
AW26	Y_G
AW27	C_R
AW28	TPVDD
AW29	TXCP
AW3	WED#
AW30	TX0P
AW31	TX1P
AW32	TX2P
AW33	VPHCTL
AW34	VID4
AW35	VID0
AW36	VPCLK0
AW37	PVDD
AW38	XTALOUT
AW4	RASD#
AW5	DQD33
AW6	DQD35
AW7	QSD4
AW8	DQD37
AW9	DQD39
B1	DQC29

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
B10	DQB48
B11	DQB38
B12	DQB36
B13	DQMB#4
B14	DQB34
B15	DQB32
B16	WEB#
B17	CSB#
B18	MAB7
B19	CLKB1
B2	VSS
B20	VSS
B21	CLKB0#
B22	DQB14
B23	DQB12
B24	DQMB#1
B25	DQB10
B26	DQB8
B27	DQB30
B28	DQB28
B29	DQMB#3
B3	DQMC#3
B30	DQB26
B31	DQB24
B32	DQA54
B33	DQA52
B34	DQMA#6
B35	DQA50
B36	DQA48
B37	DQA38
B38	DQA36
B39	QSA4
B4	DQC26
B5	DQC24
B6	DQB54
B7	DQB52
B8	DQMB#6
B9	DQB50
C1	DQC31
C10	DQMB#7
C11	DQB58
C12	DQB47
C13	VSS
C14	DQMB#5
C15	DQB42

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
C16	VSS
C17	MAB13
C18	MAB0
C19	MAB1
C2	DQC30
C20	MAB4
C21	MAB9
C22	DQB7
C23	VSS
C24	DQMB#0
C25	DQB2
C26	DQB23
C27	VSS
C28	DQMB#2
C29	DQB18
C3	VSS
C30	DQA63
C31	VSS
C32	DQMA#7
C33	DQA58
C34	DQA47
C35	VSS
C36	DQMA#5
C37	VSS
C38	DQMA#4
C39	DQA35
C4	DQC17
C5	DQC16
C6	MPVSS
C7	MPVDD
C8	DQB63
C9	VSS
D1	DQC9
D10	DQB59
D11	DQB57
D12	DQB46
D13	DQB44
D14	DQB43
D15	DQB41
D16	RASB#
D17	MAB8
D18	MAB6
D19	MAB5
D2	DQC8
D20	MAB3

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
D21	MAB10
D22	DQB6
D23	DQB4
D24	DQB3
D25	DQB1
D26	DQB22
D27	DQB20
D28	DQB19
D29	DQB17
D3	DQC19
D30	DQA62
D31	DQA60
D32	DQA59
D33	DQA57
D34	DQA46
D35	DQA44
D36	DQA43
D37	DQA41
D38	DQA34
D39	DQA33
D4	VSS
D5	DQC18
D6	VDDR1
D7	VSS
D8	DQB62
D9	DQB60
E1	DQC11
E10	VSS
E11	DQB56
E12	DQB45
E13	QSB5
E14	VSS
E15	DQB40
E16	DIMB1
E17	MAB14
E18	VSS
E19	MAB2
E2	DQC10
E20	VSS
E21	MAB11
E22	DQB5
E23	QSB0
E24	VSS
E25	DQB0
E26	DQB21

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
E27	QSB2
E28	VSS
E29	DQB16
E3	QSC2
E30	DQA61
E31	QSA7
E32	VSS
E33	DQA56
E34	DQA45
E35	QSA5
E36	DQA42
E37	DQA40
E38	DQA32
E39	CASA#
E4	DQMC#2
E5	VSS
E6	DQC20
E7	MEMVMODE0
E8	DQB61
E9	QSB7
F1	QSC1
F10	VSS
F11	VDDR1
F12	VDDR1
F13	VSS
F14	VDDR1
F15	VSS
F16	VDDR1
F17	VDDR1
F18	VSS
F19	VDDR1
F2	DQMC#1
F20	VDDR1
F21	VDDR1
F22	VDDR1
F23	VSS
F24	MEMTEST
F25	VDDR1
F26	VSS
F27	VDDR1
F28	VDDR1
F29	VSS
F3	VSS
F30	VSS
F31	VDDR1

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
F32	VDDR1
F33	VDDR1
F34	DIMA1
F35	VSS
F36	WEA#
F37	CSA#
F38	CKEA
F39	RASA#
F4	DQC22
F5	DQC21
F6	VSS
F7	MEMVMODE1
F8	VSS
F9	TEST_MCLK
G1	DQC13
G10	VDDR1
G11	VDDR1
G12	VSS
G13	VDDR1
G14	VDDR1
G15	VSS
G16	VSS
G17	VDDR1
G18	VDDR1
G19	VSS
G2	DQC12
G20	VDDC18
G21	VSSRH
G22	VDDRH
G23	VDDR1
G24	VREF2
G25	VDDR1
G26	VDDR1
G27	VSS
G28	VSS
G29	VDDR1
G3	DQC1
G30	VDDR1
G31	VSS
G32	VDDR1
G33	VDDR1
G34	MAA14
G35	MAA12
G36	MAA8
G37	MAA13

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
G38	CLKA1
G39	CLKA1#
G4	DQC0
G5	DQC23
G6	TEST_YCLK
G7	VSS
G8	VDDR1
G9	VSS
H1	DQC15
H2	DQC14
H3	DQMC#0
H33	VDDR1
H34	VDDR1
H35	MAA6
H36	MAA0
H37	MAA7
H38	VSS
H39	CLKA0
H4	DQC3
H5	DQC2
H6	VSS
H7	VDDR1
J1	DIMC0
J2	CLKC0#
J3	DQC5
J33	VDDC18
J34	VSS
J35	MAA2
J36	MAA5
J37	MAA1
J38	CLKA0#
J39	DIMA0
J4	DQC4
J5	QSC0
J6	VSS
J7	VDDR1
K1	CLKC0
K2	VSS
K3	DQC7
K33	VSS
K34	VSS
K35	VSS
K36	MAA3
K37	MAA4
K38	DQA14

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
K39	DQA15
K4	DQC6
K5	VSS
K6	VDDR1
K7	VSS
L1	CLKC1#
L2	CLKC1
L3	MAC9
L33	VDDRH
L34	VDDR1
L35	MAA11
L36	MAA10
L37	MAA9
L38	DQA12
L39	DQA13
L4	MAC10
L5	MAC11
L6	VDDR1
L7	VDDRH
M1	MAC5
M2	MAC2
M3	MAC4
M33	VSSRH
M34	VDDR1
M35	DQA5
M36	DQA6
M37	DQA7
M38	DQMA#1
M39	QSA1
M4	MAC3
M5	VDDR1
M6	VSS
M7	VSSRH
N1	MAC7
N13	VDDC
N14	VDDC
N15	VDDC
N16	VDDC
N17	VDDC
N18	VSS
N19	VSS
N2	MAC0
N20	VSS
N21	VSS
N22	VSS

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
N23	VDDCI
N24	VDDC
N25	VDDC
N26	VDDC
N27	VDDC
N3	VSS
N33	VSS
N34	VDDR1
N35	QSA0
N36	DQA4
N37	VSS
N38	DQA10
N39	DQA11
N4	MAC6
N5	MAC1
N6	VSS
N7	VDDC18
P1	DQC33
P13	VDDC
P14	VDDC
P15	VDDC
P16	VDDC
P17	VDDC
P18	VSS
P19	VSS
P2	DQC32
P20	VSS
P21	VSS
P22	VSS
P23	VDDC
P24	VDDC
P25	VDDC
P26	VDDC
P27	VDDC
P3	MAC13
P33	VSS
P34	VSS
P35	VSS
P36	DQA3
P37	DQMA#0
P38	DQA8
P39	DQA9
P4	MAC8
P5	MAC12
P6	MAC14

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
P7	VSS
R1	DQC35
R13	VDDC
R14	VDDC
R15	VDDC
R16	VDDC
R17	VDDC
R18	VSS
R19	VSS
R2	DQC34
R20	VSS
R21	VSS
R22	VSS
R23	VDDC
R24	VDDC
R25	VDDC
R26	VDDC
R27	VDDC
R3	CSC#
R33	VDDR1
R34	VSS
R35	DQA0
R36	DQA1
R37	DQA2
R38	DQA30
R39	DQA31
R4	RASC#
R5	CKEC
R6	VDDR1
R7	VSS
T1	QSC4
T13	VDDC
T14	VDDC
T15	VDDC
T16	VDDC
T17	VDDC
T18	VSS
T19	VSS
T2	DQMC#4
T20	VSS
T21	VSS
T22	VSS
T23	VDDC
T24	VDDC
T25	VDDC

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
T26	VDDC
T27	VDDC
T3	VSS
T33	VDDR1
T34	VDDR1
T35	DQA21
T36	DQA22
T37	DQA23
T38	DQA28
T39	DQA29
T4	CASC#
T5	WEC#
T6	VSS
T7	VDDR1
U1	DQC37
U13	VDDC
U14	VDDC
U15	VDDC
U16	VDDC
U17	VDDC
U18	VSS
U19	VSS
U2	DQC36
U20	VSS
U21	VSS
U22	VSS
U23	VDDC
U24	VDDC
U25	VDDC
U26	VDDC
U27	VDDC
U3	DQC41
U33	VSS
U34	VDDR1
U35	QSA2
U36	DQA20
U37	VSS
U38	DQMA#3
U39	QSA3
U4	DQC40
U5	DIMC1
U6	VSS
U7	VDDR1
V1	DQC39
V13	VSS

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
V14	VSS
V15	VSS
V16	VSS
V17	VSS
V18	VSS
V19	VSS
V2	DQC38
V20	VSS
V21	VSS
V22	VSS
V23	VSS
V24	VSS
V25	VSS
V26	VSS
V27	VSS
V3	DQMC#5
V33	VDDR1
V34	VSS
V35	VSS
V36	DQA19
V37	DQMA#2
V38	DQA26
V39	DQA27
V4	DQC43
V5	DQC42
V6	VDDR1
V7	VDDR1
W1	DQC49
W13	VSS
W14	VSS
W15	VSS
W16	VSS
W17	VSS
W18	VSS
W19	VSS
W2	DQC48
W20	VSS
W21	VSS
W22	VSS
W23	VSS
W24	VSS
W25	VSS
W26	VSS
W27	VSS
W3	DQC44

Table A-1 RADEON 9800 Pin List Sorted by Ball Reference (Cont'd)

Ball Ref	Signal
W33	VDDR1
W34	VDDR1
W35	DQA16
W36	DQA17
W37	DQA18
W38	DQA24
W39	DQA25
W4	QSC5
W5	VSS
W6	VDDR1
W7	VSS
Y1	DQC51
Y13	VSS
Y14	VSS
Y15	VSS
Y16	VSS
Y17	VSS
Y18	VSS
Y19	VSS
Y2	DQC50
Y20	VSS
Y21	VSS
Y22	VSS
Y23	VSS
Y24	VSS
Y25	VSS
Y26	VSS
Y27	VSS
Y3	VSS
Y33	VDDP
Y34	VSSP
Y35	VSSP
Y36	AD0
Y37	AD1
Y38	VSSP
Y39	AD16
Y4	DQC46
Y5	DQC45
Y6	VSS
Y7	VSS

A.2 RADEON 9800 Pin List Sorted by Signal Name

Table A-2 RADEON 9800 Pin List Sorted by Signal Name

Ball Ref	Signal
AV26	A2VDD1
AV27	A2VDD2
AU25	A2VDDQ
AT25	A2VSSN1
AU26	A2VSSN2
AT27	A2VSSQ
AE37	AD_STBF0
AF39	AD_STBF1
AD36	AD_STBS0
AE38	AD_STBS1
Y36	AD0
Y37	AD1
AG37	AD10
AH36	AD11
AH37	AD12
AJ36	AD13
AK37	AD14
AK36	AD15
Y39	AD16
AB39	AD17
AA38	AD18
AC39	AD19
AA36	AD2
AB38	AD20
AD39	AD21
AC38	AD22
AE39	AD23
AG39	AD24
AG38	AD25
AH39	AD26
AH38	AD27
AJ39	AD28
AJ38	AD29
AA37	AD3
AK39	AD30
AK38	AD31
AB36	AD4
AB37	AD5
AC36	AD6
AD37	AD7
AF37	AD8
AG36	AD9

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
AL35	AGP8X_DET#
AG34	AGPREF
AL36	AGPTEST
AP31	AUXWIN
AV23	AVDD1
AV24	AVDD2
AR24	AVSSN1
AT24	AVSSN2
AU22	AVSSQ
AW22	B
AW27	C_R
E39	CASA#
A16	CASB#
T4	CASC#
AW2	CASD#
AF36	CBE#0
AL37	CBE#1
AA39	CBE#2
AD38	CBE#3
F38	CKEA
A17	CKEB
R5	CKEC
AV1	CKED
H39	CLKA0
J38	CLKA0#
G38	CLKA1
G39	CLKA1#
A20	CLKB0
B21	CLKB0#
B19	CLKB1
A19	CLKB1#
K1	CLKC0
J2	CLKC0#
L2	CLKC1
L1	CLKC1#
AR1	CLKD0
AP2	CLKD0#
AT2	CLKD1
AT1	CLKD1#
AW25	COMP_B
F37	CSA#
B17	CSB#
R3	CSC#
AV3	CSD#
AL38	DBI_HI

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
AL39	DBI_LO
AU31	DDC1CLK
AU32	DDC1DATA
AR34	DDC2CLK
AR35	DDC2DATA
AD35	DEVSEL#
J39	DIMA0
F34	DIMA1
A21	DIMB0
E16	DIMB1
J1	DIMC0
U5	DIMC1
AP1	DIMD0
AR7	DIMD1
R35	DQA0
R36	DQA1
N38	DQA10
N39	DQA11
L38	DQA12
L39	DQA13
K38	DQA14
K39	DQA15
W35	DQA16
W36	DQA17
W37	DQA18
V36	DQA19
R37	DQA2
U36	DQA20
T35	DQA21
T36	DQA22
T37	DQA23
W38	DQA24
W39	DQA25
V38	DQA26
V39	DQA27
T38	DQA28
T39	DQA29
P36	DQA3
R38	DQA30
R39	DQA31
E38	DQA32
D39	DQA33
D38	DQA34
C39	DQA35
B38	DQA36

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
A38	DQA37
B37	DQA38
A37	DQA39
N36	DQA4
E37	DQA40
D37	DQA41
E36	DQA42
D36	DQA43
D35	DQA44
E34	DQA45
D34	DQA46
C34	DQA47
B36	DQA48
A36	DQA49
M35	DQA5
B35	DQA50
A35	DQA51
B33	DQA52
A33	DQA53
B32	DQA54
A32	DQA55
E33	DQA56
D33	DQA57
C33	DQA58
D32	DQA59
M36	DQA6
D31	DQA60
E30	DQA61
D30	DQA62
C30	DQA63
M37	DQA7
P38	DQA8
P39	DQA9
E25	DQB0
D25	DQB1
B25	DQB10
A25	DQB11
B23	DQB12
A23	DQB13
B22	DQB14
A22	DQB15
E29	DQB16
D29	DQB17
C29	DQB18
D28	DQB19

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
C25	DQB2
D27	DQB20
E26	DQB21
D26	DQB22
C26	DQB23
B31	DQB24
A31	DQB25
B30	DQB26
A30	DQB27
B28	DQB28
A28	DQB29
D24	DQB3
B27	DQB30
A27	DQB31
B15	DQB32
A15	DQB33
B14	DQB34
A14	DQB35
B12	DQB36
A12	DQB37
B11	DQB38
A11	DQB39
D23	DQB4
E15	DQB40
D15	DQB41
C15	DQB42
D14	DQB43
D13	DQB44
E12	DQB45
D12	DQB46
C12	DQB47
B10	DQB48
A10	DQB49
E22	DQB5
B9	DQB50
A9	DQB51
B7	DQB52
A7	DQB53
B6	DQB54
A6	DQB55
E11	DQB56
D11	DQB57
C11	DQB58
D10	DQB59
D22	DQB6

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
D9	DQB60
E8	DQB61
D8	DQB62
C8	DQB63
C22	DQB7
B26	DQB8
A26	DQB9
G4	DQC0
G3	DQC1
E2	DQC10
E1	DQC11
G2	DQC12
G1	DQC13
H2	DQC14
H1	DQC15
C5	DQC16
C4	DQC17
D5	DQC18
D3	DQC19
H5	DQC2
E6	DQC20
F5	DQC21
F4	DQC22
G5	DQC23
B5	DQC24
A5	DQC25
B4	DQC26
A4	DQC27
A2	DQC28
B1	DQC29
H4	DQC3
C2	DQC30
C1	DQC31
P2	DQC32
P1	DQC33
R2	DQC34
R1	DQC35
U2	DQC36
U1	DQC37
V2	DQC38
V1	DQC39
J4	DQC4
U4	DQC40
U3	DQC41
V5	DQC42

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
V4	DQC43
W3	DQC44
Y5	DQC45
Y4	DQC46
AA5	DQC47
W2	DQC48
W1	DQC49
J3	DQC5
Y2	DQC50
Y1	DQC51
AB2	DQC52
AB1	DQC53
AC2	DQC54
AC1	DQC55
AA4	DQC56
AA3	DQC57
AB5	DQC58
AB4	DQC59
K4	DQC6
AC3	DQC60
AD5	DQC61
AD4	DQC62
AE5	DQC63
K3	DQC7
D2	DQC8
D1	DQC9
AJ4	DQD0
AJ3	DQD1
AK2	DQD10
AK1	DQD11
AM2	DQD12
AM1	DQD13
AN2	DQD14
AN1	DQD15
AE4	DQD16
AE3	DQD17
AF5	DQD18
AF4	DQD19
AK5	DQD2
AG3	DQD20
AH5	DQD21
AH4	DQD22
AJ5	DQD23
AD2	DQD24
AD1	DQD25

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
AE2	DQD26
AE1	DQD27
AG2	DQD28
AG1	DQD29
AK4	DQD3
AH2	DQD30
AH1	DQD31
AV5	DQD32
AW5	DQD33
AV6	DQD34
AW6	DQD35
AV8	DQD36
AW8	DQD37
AV9	DQD38
AW9	DQD39
AL3	DQD4
AT7	DQD40
AU7	DQD41
AR8	DQD42
AT8	DQD43
AT9	DQD44
AR10	DQD45
AT10	DQD46
AU10	DQD47
AV10	DQD48
AW10	DQD49
AM5	DQD5
AV11	DQD50
AW11	DQD51
AV13	DQD52
AW13	DQD53
AV14	DQD54
AW14	DQD55
AR11	DQD56
AT11	DQD57
AU11	DQD58
AT12	DQD59
AM4	DQD6
AT13	DQD60
AR14	DQD61
AT14	DQD62
AU14	DQD63
AN5	DQD7
AJ2	DQD8
AJ1	DQD9

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
P37	DQMA#0
M38	DQMA#1
V37	DQMA#2
U38	DQMA#3
C38	DQMA#4
C36	DQMA#5
B34	DQMA#6
C32	DQMA#7
C24	DQMB#0
B24	DQMB#1
C28	DQMB#2
B29	DQMB#3
B13	DQMB#4
C14	DQMB#5
B8	DQMB#6
C10	DQMB#7
H3	DQMC#0
F2	DQMC#1
E4	DQMC#2
B3	DQMC#3
T2	DQMC#4
V3	DQMC#5
AA2	DQMC#6
AB3	DQMC#7
AK3	DQMD#0
AL2	DQMD#1
AF3	DQMD#2
AF2	DQMD#3
AV7	DQMD#4
AU8	DQMD#5
AV12	DQMD#6
AU12	DQMD#7
AU36	DVALID
AW17	DVOCLK0
AV17	DVOCLK1
AU15	DVOCNTL0
AV15	DVOCNTL1
AW15	DVOCNTL2
AT15	DVODATA0
AR15	DVODATA1
AV18	DVODATA10
AU18	DVODATA11
AW16	DVODATA2
AV16	DVODATA3
AU16	DVODATA4

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
AT16	DVODATA5
AU17	DVODATA6
AT17	DVODATA7
AR17	DVODATA8
AW18	DVODATA9
AT18	DVOVMODE
AG35	FRAME#
AW23	G
AP38	GNT#
AR32	H2SYNC
AR31	HPD1
AR33	HPD2
AT31	HSYNC
AU37	INTA#
AH35	IRDY#
H36	MAA0
J37	MAA1
L36	MAA10
L35	MAA11
G35	MAA12
G37	MAA13
G34	MAA14
J35	MAA2
K36	MAA3
K37	MAA4
J36	MAA5
H35	MAA6
H37	MAA7
G36	MAA8
L37	MAA9
C18	MAB0
C19	MAB1
D21	MAB10
E21	MAB11
A18	MAB12
C17	MAB13
E17	MAB14
E19	MAB2
D20	MAB3
C20	MAB4
D19	MAB5
D18	MAB6
B18	MAB7
D17	MAB8
C21	MAB9

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
N2	MAC0
N5	MAC1
L4	MAC10
L5	MAC11
P5	MAC12
P3	MAC13
P6	MAC14
M2	MAC2
M4	MAC3
M3	MAC4
M1	MAC5
N4	MAC6
N1	MAC7
P4	MAC8
L3	MAC9
AT3	MAD0
AT6	MAD1
AN3	MAD10
AN4	MAD11
AU4	MAD12
AU1	MAD13
AV4	MAD14
AR4	MAD2
AP3	MAD3
AR6	MAD4
AR3	MAD5
AT5	MAD6
AU5	MAD7
AU2	MAD8
AP4	MAD9
F24	MEMTEST
E7	MEMVMODE0
F7	MEMVMODE1
C7	MPVDD
C6	MPVSS
AA35	PAR
AV39	PCICLK
AV36	PSYNC
AW37	PVDD
AV37	PVSS
N35	QSA0
M39	QSA1
U35	QSA2
U39	QSA3
B39	QSA4

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
E35	QSA5
A34	QSA6
E31	QSA7
E23	QSB0
A24	QSB1
E27	QSB2
A29	QSB3
A13	QSB4
E13	QSB5
A8	QSB6
E9	QSB7
J5	QSC0
F1	QSC1
E3	QSC2
A3	QSC3
T1	QSC4
W4	QSC5
AA1	QSC6
AC4	QSC7
AL4	QSD0
AL1	QSD1
AG4	QSD2
AF1	QSD3
AW7	QSD4
AR9	QSD5
AW12	QSD6
AR13	QSD7
AW24	R
AV25	R2SET
F39	RASA#
D16	RASB#
R4	RASC#
AW4	RASD#
AM39	RBF#
AU39	REQ#
AR30	ROMCS#
AP30	ROMSCK
AR29	ROMSI
AP29	ROMSO
AV22	RSET
AP35	RST#
AR38	SB_STBF
AR37	SB_STBS
AT37	SBA0
AT38	SBA1

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
AT39	SBA2
AR39	SBA3
AP36	SBA4
AP37	SBA5
AN36	SBA6
AN37	SBA7
AR27	SCL
AR28	SDA
AP39	ST0
AN39	ST1
AN38	ST2
AP32	STEREOSYNC
AB35	STOP#
AP33	TEST_AGPCLK
F9	TEST_MCLK
G6	TEST_YCLK
AT36	TESTEN
AW28	TPVDD
AV28	TPVSS
AE35	TRDY#
AV21	TVOCLKI
AW21	TVOCLKO
AW19	TVODATA0
AV19	TVODATA1
AU19	TVODATA2
AT19	TVODATA3
AW20	TVODATA4
AV20	TVODATA5
AU20	TVODATA6
AT20	TVODATA7
AU21	TVODATA8
AT21	TVODATA9
AR19	TVOVMODE
AV30	TX0M
AW30	TX0P
AV31	TX1M
AW31	TX1P
AV32	TX2M
AW32	TX2P
AV29	TXCM
AW29	TXCP
AT29	TXVDDR1
AT28	TXVDDR2
AU28	TXVSSR1
AU29	TXVSSR2

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
AU30	TXVSSR3
AT32	V2SYNC
AU23	VDD1DI
AU27	VDD2DI
R13	VDDC
T25	VDDC
T26	VDDC
T27	VDDC
U23	VDDC
U24	VDDC
U25	VDDC
U26	VDDC
U27	VDDC
AC14	VDDC
T13	VDDC
AC15	VDDC
AC16	VDDC
AC17	VDDC
AD13	VDDC
AD14	VDDC
AD15	VDDC
AD16	VDDC
AD17	VDDC
AE13	VDDC
AE14	VDDC
U13	VDDC
AE15	VDDC
AE16	VDDC
AE17	VDDC
AF13	VDDC
AF14	VDDC
AF15	VDDC
AF16	VDDC
AF17	VDDC
AG13	VDDC
AG14	VDDC
N14	VDDC
AG15	VDDC
AG16	VDDC
AG17	VDDC
N15	VDDC
P14	VDDC
R14	VDDC
T14	VDDC
U14	VDDC

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
P15	VDDC
AV2	VDDC
R15	VDDC
T15	VDDC
U15	VDDC
N16	VDDC
P16	VDDC
R16	VDDC
T16	VDDC
U16	VDDC
N17	VDDC
P17	VDDC
AU3	VDDC
R17	VDDC
T17	VDDC
U17	VDDC
AT4	VDDC
AR5	VDDC
AC23	VDDC
AD23	VDDC
AP6	VDDC
AE23	VDDC
AF23	VDDC
AC24	VDDC
AD24	VDDC
AE24	VDDC
AF24	VDDC
AG24	VDDC
AC25	VDDC
AD25	VDDC
AN7	VDDC
AE25	VDDC
AF25	VDDC
AG25	VDDC
AC26	VDDC
AD26	VDDC
AE26	VDDC
AF26	VDDC
AG26	VDDC
AD27	VDDC
N13	VDDC
AE27	VDDC
AF27	VDDC
AG27	VDDC
N24	VDDC

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
N25	VDDC
N26	VDDC
N27	VDDC
P23	VDDC
P24	VDDC
P13	VDDC
P25	VDDC
P26	VDDC
P27	VDDC
R23	VDDC
R24	VDDC
R25	VDDC
R26	VDDC
R27	VDDC
T23	VDDC
T24	VDDC
J33	VDDC18
N7	VDDC18
AK7	VDDC18
G20	VDDC18
AN22	VDDC18
AN27	VDDC18
AN32	VDDC18
AC27	VDDCI
AG23	VDDCI
AC13	VDDCI
N23	VDDCI
AN34	VDDP
AL33	VDDP
AJ34	VDDP
AF34	VDDP
AB34	VDDP
AH33	VDDP
AG33	VDDP
AF33	VDDP
AE33	VDDP
AM34	VDDP
AD33	VDDP
AN33	VDDP
AK33	VDDP
AJ33	VDDP
AC33	VDDP
AB33	VDDP
AA33	VDDP
Y33	VDDP

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
M34	VDDR1
W33	VDDR1
W34	VDDR1
F11	VDDR1
F28	VDDR1
G13	VDDR1
F14	VDDR1
F16	VDDR1
F17	VDDR1
G23	VDDR1
F33	VDDR1
F25	VDDR1
F27	VDDR1
T34	VDDR1
F31	VDDR1
G8	VDDR1
G26	VDDR1
G10	VDDR1
G11	VDDR1
G17	VDDR1
G18	VDDR1
H33	VDDR1
F19	VDDR1
F20	VDDR1
F21	VDDR1
F22	VDDR1
G25	VDDR1
G29	VDDR1
G30	VDDR1
R33	VDDR1
G32	VDDR1
H7	VDDR1
R6	VDDR1
K6	VDDR1
J7	VDDR1
L6	VDDR1
T7	VDDR1
V6	VDDR1
V7	VDDR1
W6	VDDR1
AF7	VDDR1
D6	VDDR1
U34	VDDR1
AA6	VDDR1
AA7	VDDR1

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
AB7	VDDR1
AB6	VDDR1
AE6	VDDR1
AD6	VDDR1
AG7	VDDR1
AJ6	VDDR1
AP8	VDDR1
L34	VDDR1
AP12	VDDR1
AN6	VDDR1
AL6	VDDR1
AN8	VDDR1
AN12	VDDR1
AP11	VDDR1
AN13	VDDR1
AN9	VDDR1
AP10	VDDR1
G14	VDDR1
N34	VDDR1
F12	VDDR1
AN14	VDDR1
F32	VDDR1
H34	VDDR1
G33	VDDR1
M5	VDDR1
U7	VDDR1
AM6	VDDR1
AP7	VDDR1
T33	VDDR1
V33	VDDR1
AP19	VDDR2
AN21	VDDR2
AP20	VDDR2
AR25	VDDR3
AN29	VDDR3
AP26	VDDR3
AN28	VDDR3
AN25	VDDR3
AR22	VDDR3
AR23	VDDR3
AP24	VDDR3
AP27	VDDR3
AN17	VDDR4
AN18	VDDR4
AP15	VDDR4

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
AR16	VDDR4
AP16	VDDR4
L33	VDDRH
G22	VDDRH
L7	VDDRH
AL7	VDDRH
AU33	VHAD0
AT33	VHAD1
AW35	VID0
AV35	VID1
AU35	VID2
AT35	VID3
AW34	VID4
AV34	VID5
AU34	VID6
AT34	VID7
AV33	VIPCLK
AW36	VPCLK0
AW33	VPHCTL
AC6	VREF1
G24	VREF2
AB17	VSS
V18	VSS
W18	VSS
Y18	VSS
AA18	VSS
AB18	VSS
V19	VSS
W19	VSS
Y19	VSS
AA19	VSS
AB19	VSS
V20	VSS
W20	VSS
Y20	VSS
AA20	VSS
AB20	VSS
V21	VSS
W21	VSS
Y21	VSS
AA21	VSS
AB21	VSS
V22	VSS
W22	VSS
Y22	VSS

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
AA22	VSS
AB22	VSS
N18	VSS
P18	VSS
R18	VSS
T18	VSS
U18	VSS
N19	VSS
P19	VSS
R19	VSS
T19	VSS
U19	VSS
N20	VSS
P20	VSS
R20	VSS
T20	VSS
U20	VSS
N21	VSS
P21	VSS
R21	VSS
T21	VSS
U21	VSS
N22	VSS
P22	VSS
R22	VSS
T22	VSS
U22	VSS
V23	VSS
W23	VSS
Y23	VSS
AA23	VSS
AB23	VSS
V24	VSS
W24	VSS
Y24	VSS
AA24	VSS
AB24	VSS
V25	VSS
W25	VSS
Y25	VSS
AA25	VSS
AB25	VSS
V26	VSS
W26	VSS
AB26	VSS

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
V27	VSS
W27	VSS
Y27	VSS
AA27	VSS
AB27	VSS
AP28	VSS
AR26	VSS
AG22	VSS
AT22	VSS
AP34	VSS
AR20	VSS
AT23	VSS
AR21	VSS
AN31	VSS
AF22	VSS
AA26	VSS
AN23	VSS
AP25	VSS
AE22	VSS
AN30	VSS
AD22	VSS
AP22	VSS
AP17	VSS
AR18	VSS
AN19	VSS
AP21	VSS
AC22	VSS
AC21	VSS
AN24	VSS
AN16	VSS
AK6	VSS
AN10	VSS
AN15	VSS
AN20	VSS
AP13	VSS
AP14	VSS
AP18	VSS
AP9	VSS
AN11	VSS
AH7	VSS
AJ7	VSS
AP23	VSS
AF6	VSS
AG6	VSS
AD7	VSS

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
Y6	VSS
W7	VSS
M6	VSS
Y7	VSS
R7	VSS
P7	VSS
T6	VSS
K7	VSS
Y26	VSS
G12	VSS
F10	VSS
G9	VSS
F13	VSS
F15	VSS
G19	VSS
G15	VSS
G16	VSS
F18	VSS
F23	VSS
U37	VSS
AN26	VSS
AC7	VSS
F26	VSS
G27	VSS
G28	VSS
F30	VSS
G31	VSS
J34	VSS
K34	VSS
K33	VSS
U33	VSS
J6	VSS
N33	VSS
F35	VSS
P34	VSS
V34	VSS
R34	VSS
P33	VSS
F29	VSS
AC18	VSS
AD18	VSS
AE18	VSS
AF18	VSS
AG18	VSS
AG19	VSS

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
AF19	VSS
AE19	VSS
P35	VSS
AD19	VSS
AC19	VSS
AC20	VSS
AD20	VSS
AE20	VSS
AF20	VSS
AG20	VSS
AG21	VSS
AF21	VSS
AE21	VSS
V35	VSS
AD21	VSS
F8	VSS
H6	VSS
D7	VSS
F3	VSS
V13	VSS
N37	VSS
T3	VSS
C37	VSS
H38	VSS
K35	VSS
U6	VSS
W13	VSS
C35	VSS
C31	VSS
E32	VSS
E28	VSS
C27	VSS
Y13	VSS
AA13	VSS
E24	VSS
G7	VSS
E20	VSS
AB13	VSS
V14	VSS
C16	VSS
E18	VSS
C23	VSS
B20	VSS
E14	VSS
D4	VSS

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
C13	VSS
E5	VSS
C9	VSS
E10	VSS
C3	VSS
K2	VSS
N6	VSS
AD3	VSS
AP5	VSS
AH3	VSS
N3	VSS
W5	VSS
Y3	VSS
AU9	VSS
AM3	VSS
K5	VSS
AC5	VSS
AU13	VSS
W14	VSS
AL5	VSS
B2	VSS
AR2	VSS
AU6	VSS
Y14	VSS
F6	VSS
AR12	VSS
AA14	VSS
AB14	VSS
V15	VSS
W15	VSS
Y15	VSS
AA15	VSS
AB15	VSS
V16	VSS
W16	VSS
Y16	VSS
AA16	VSS
AB16	VSS
V17	VSS
W17	VSS
Y17	VSS
AA17	VSS
AE7	VSS
AU24	VSS1DI
AT26	VSS2DI

Table A-2 RADEON 9800 Pin List Sorted by Signal Name (Cont'd)

Ball Ref	Signal
AU38	VSSP
AM35	VSSP
AJ35	VSSP
AF35	VSSP
Y35	VSSP
AM33	VSSP
AL34	VSSP
AN35	VSSP
AK34	VSSP
AH34	VSSP
AM38	VSSP
AE34	VSSP
AD34	VSSP
AC34	VSSP
AA34	VSSP
Y34	VSSP
AC35	VSSP
AK35	VSSP
AF38	VSSP
Y38	VSSP
AM37	VSSP
AJ37	VSSP
AC37	VSSP
AR36	VSSP
AE36	VSSP
M33	VSSRH
G21	VSSRH
M7	VSSRH
AM7	VSSRH
AT30	VSYNC
AG5	VT1
AH6	VT2
AM36	WBF#
F36	WEA#
B16	WEB#
T5	WEC#
AW3	WED#
AV38	XTALIN
AW38	XTALOUT
AW26	Y_G

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Appendix B
Revision History

Note: Two release states are defined:

Preliminary Release — Revision numbers from 0.1 to 0.9, generally with incomplete information and/or information subject to change.

Full Release — Revision numbers from 1.0 onwards, occuring after the essential elements have been reviewed (typically after tape-out).

Rev 0.1 (Feb 2003)

- First release.

Rev 0.2 (Mar 2003)

- Added section 1.3 Branding Diagram.
- Updated section 2.7 3D Features.
- Modified section 3.7 Six PLL Clock Synthesizer.
- Modified section 3.10.1 Memory Configurations.
- Updated Table 5-9 Memory Interface Electrical Characteristics SSTL.
- Updated section 5.2.1 Maximum Ambient Temperature and Case Temperature and section 5.2.2 Heat Sink Selection.
- General edits.

Rev 0.3 (May 2003)

- Updated Table 1-1 RADEON 9800 Series Component Part Numbers.
- Modified section 1.3 Branding Diagram.
- Modified description of TMDS in section 2.5.3 Display Output Features.

Rev 0.4 (July 2003)

- Updated Table 1-1 RADEON 9800 Series Component Part Numbers.
- Updated RADEON 9800 mechanical drawing in section 5.3 Physical Dimensions.

Rev 0.5 (Aug 2003)

- Added R360 bin 1 and bin 2 variants.
- Updated Table 1-1 RADEON 9800 Series Component Part Numbers.
- Modified Table 2-1 2D Performance.
- Updated section 2.8 3D Features.
- Modified section 2.9 Compliance with Wassenaar Agreement.
- Updated section 3.7 Six PLL Clock Synthesizer.
- Edited section 3.10.1 Memory Configurations.
- Modified Table 4-26 Core Power.
- Updated section 5.2.1 Maximum Ambient Temperature and Case Temperature.
- Modified section 5.2.2 Heat Sink Selection.
- Edited Table 5-2 Recommended DC Operating Conditions.
- Modified section 5.2.1 Maximum Ambient Temperature and Case Temperature and section 5.2.2 Heat Sink Selection.

Rev 0.6 (Aug 2003)

- Divided Chapter 5 Electrical Characteristics and Physical Data into 3 chapters: Chapter 5 Electrical Characteristics, Chapter 6 Thermal Data, and Chapter 7 Mechanical Data.

- Updated mechanical drawing for RADEON 9800 Series in Chapter 7 Mechanical Data.

Rev 1.0 (Nov 2003)

- Clarified external TMDS support (removed SDR support) in section 2.5.3 “Display Output Features” on page 2-2..
- Reorganized Chapter 5 Electrical Characteristics (consolidated the DAC section, modified RSET/R2SET calculation formula).
- Added section 6.2 “R360/R350 Power Dissipation” on page 6-2. and section 6.3 “ASIC Case Temperature and Junction Temperature” on page 6-5.

Rev 1.1 (Jan 2005)

- Added ATI vendor ID to section 1.2 “RADEON 9800 Variants” on page 1-2.
- Updated Table 1-1, “RADEON 9800 Series Component Part Numbers,” on page 1-2.